Exhibit 3

[redacted]

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Paper 51
Entered: December 5, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00999
Patent 11,232,054 B2

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and DANIEL J. GALLIGAN, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00405 and have been joined as petitioners in this proceeding. *See* Paper 27.

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. ("Samsung") filed a Petition (Paper 1, "Pet.") for *inter partes* review of claims 1–30 ("challenged claims") of U.S. Patent 11,232,054 B2 (Ex. 1001, "the '054 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.") to the Petition. We instituted *inter partes* review under 35 U.S.C. § 314(a). Paper 11 ("Inst. Dec.").

During the trial, Patent Owner filed a Response (Paper 22, "Resp."), Petitioner filed a Reply (Paper 26), and Patent Owner filed a Sur-Reply (Paper 33). We joined Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC as petitioners in this proceeding, and we refer to Samsung and these entities collectively as "Petitioner." *See* Paper 27.

Petitioner and Patent Owner requested oral argument (Papers 29 and 30). A hearing was conducted on September 11, 2023. Paper 49 ("Tr.").

Petitioner objected to evidence (Papers 23, 34) and filed a Motion to Exclude (Paper 35). Patent Owner filed an Opposition to Petitioner's Motion to Exclude (Paper 36), and Petitioner filed a Reply (Paper 39) in support of its Motion to Exclude.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). Having reviewed the complete trial record, we determine that Petitioner has shown, by a preponderance of the evidence, that the challenged claims are unpatentable.

B. Real Parties in Interest

Petitioner entities, Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC identify themselves as real parties in interest. Pet. 1; IPR2023-00405, Paper 3, 1.

Patent Owner identifies itself as the sole real party in interest. Paper 4, 1.

C. Related Matters

The parties advise that the '054 patent is related to the following pending matters:

- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.,* No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
- IPR2012-00996 (U.S. Patent No. 11,016,918)
- IPR2017-00692 (U.S. Patent No. 8,874,831)
- U.S. Patent Application No. 17/582,797

Pet. 1; Paper 4, 1.

D. Overview of the '054 Patent (Ex. 1001)

The '054 patent is titled "Flash-DRAM Hybrid Memory Module." Ex. 1001, code (54). Figure 12 of the '054 patent is reproduced below.

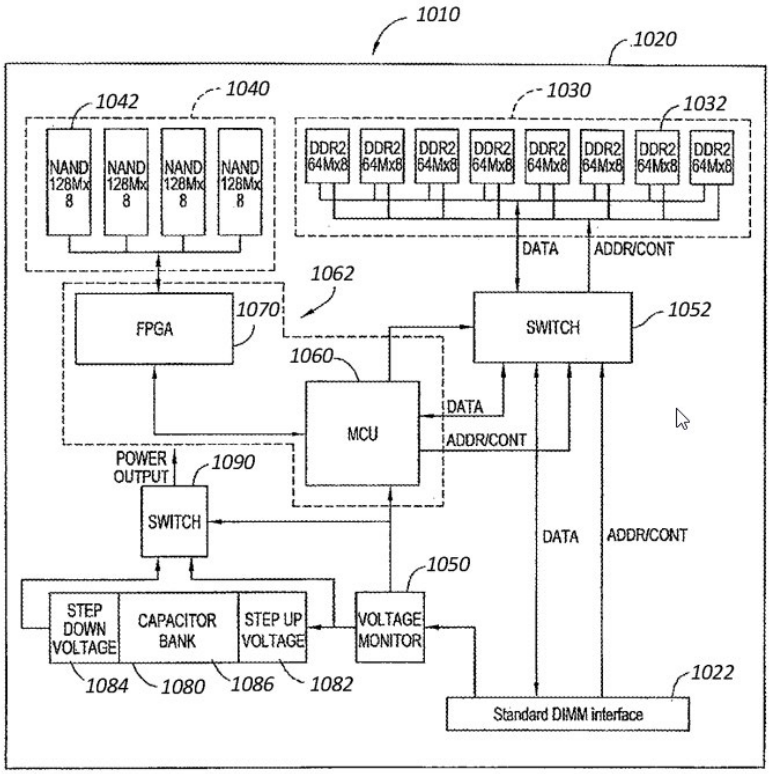


FIG. 12

Figure 12 shows an example memory system 1010 of the '054 patent. *Id.* at 21:14–16. The memory system 1010 includes a volatile memory subsystem 1030, a non-volatile memory subsystem 1040, and a controller 1062 operatively coupled to the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. *Id.* at 21:16–20. Volatile memory 1030 may comprise elements 1032 of two or more dynamic random access memory (DRAM) elements such as double data rate (DDR), DDR2, DDR3, and synchronous DRAM (SDRAM). *Id.* at 22:16–19. Non-volatile memory 1040 may comprise elements 1042 of flash memory elements such as NOR, NAND, ONE-NAND flash and multi-level cell (MLC). *Id.* at 22:35–40. Memory system 1010 may comprise a memory module or printed circuit board 1020. *Id.* at 21:24–26. Memory system 1010 has an interface 1022

for power voltage, data, address, and control signal transfer between memory system 1010 and a host system. *Id.* at 22:3–6.

Controller 1062 may include microcontroller unit 1060 and FPGA logic 1070, either as separate devices or integrated together. Ex. 1001, 24:35–37, 23:19–22, Fig. 14. Microcontroller 1060 may transfer data between the volatile memory 1030 and non-volatile memory 1040. *Id.* at 24:35–41. Logic element 1070 provides signal level translation and address translation between the volatile memory and the non-volatile memory. *Id.* at 24:45–56.

When the system is operating normally, controller 1062 controls switch 1052 to decouple the volatile memory 1030 from controller 1062 and the non-volatile memory 1040 (the '054 patent refers to this as the "first state"). *Id.* at 24:60–25:7. In response to a power interruption, for example, controller 1062 controls switch 1052 to couple the volatile memory 1030 to itself and non-volatile memory 1040, and transfers data from the volatile memory to the non-volatile memory to prevent its loss (the '054 patent refers to this as the "second state"). *Id.* at 25:9–20.

Memory system 1010 may comprise a voltage monitor 1050 to monitor voltage supplied from the host system via interface 1022. *Id.* at 25:8–10. When the voltage monitor 1050 detects a low voltage condition, the voltage monitor transmits a signal to the controller 1062 to indicate the detected condition. *Id.* at 25:11–15.

Power may be supplied from a first power supply (e.g. a system power supply) when the memory system 1010 is in the first state and from a second power supply 1080 when the memory system 1010 is in the second state. *Id.* at 25:54–58. Second power supply 1080 may comprise step-up transformer

1082, step-down transformer 1084, and capacitor bank 1086 with one or more capacitors. *Id.* at 26:3–13.

The memory system 1010 further has a third state in which controller 1062 is decoupled from the volatile memory system 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). *Id.* at 25:62–66. The third power supply may provide power to volatile memory subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred. *Id.* at 25:66–26:3.

Figure 16 of the '054 patent is reproduced below.

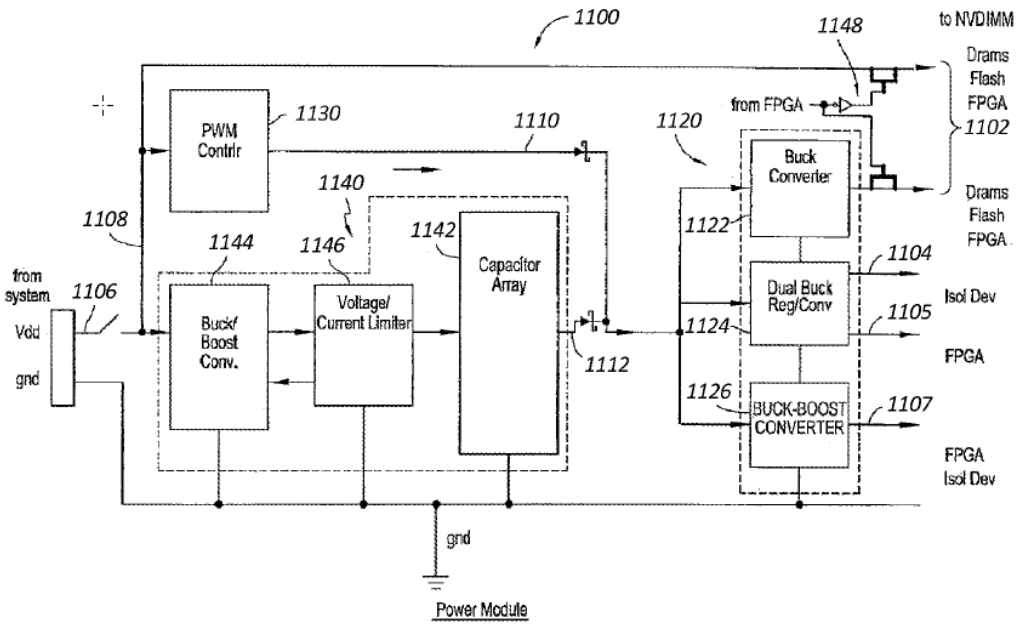


FIG. 16

Figure 16 shows power module 1100 of memory system 1010. Ex. 1001, 27:59–61. Power module 1100 comprises conversion element 1120, first power element 1130, and second power element 1140. *Id.* at 28:7–15, 28:20–22. Conversion element 1120 comprises buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 generating respective

voltages 1102, 1104, 1105, 1107 from the outputs of the first and second power elements 1130, 1140. *Id.* at 28:62–67. The first power element 1130 may comprise a pulse-width modulation power controller generating voltage 1110 from voltages 1106, 1108. *Id.* at 28:13–15. Second power element 1140 may comprise capacitor array 1142, buck-boost converter 1144 receiving voltages 1106, 1108 and adjusting the voltage for charging the capacitor array, and voltage/current limiter 1146, which limits charge current to the capacitor array and stops charging the capacitor array 1142 when it reaches a certain charge voltage. *Id.* at 28:62–67. Power module 1100 provides power to components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition. *Id.* at 27:61–65.

Specifically, in a first state, first voltage 1102 is provided to memory system 1010 from input 1106 and fourth voltage 1102 is provided to conversion element 1120 from the first power element 1130. Ex. 1001, 28:27–31. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120. *Id.* at 28:31–34. In the third state, the fifth voltage is provided to conversion element 1120 from second power element 1140 and the first voltage 1104 is provided to memory system 1010 from conversion element 1120. *Id.* at 28:34–38. Transition from the first state to the second state may occur when power module 1100 detects a power failure is about to occur, and transition from the second state to the third state may occur when it detects a power failure has occurred. *Id.* at 28:39–47.

E. Illustrative Claim

Of the challenged claims, claims 1, 16, and 24 are independent. Independent claim 1, reproduced below with brackets noting Petitioner's identifiers, is illustrative of the claimed subject matter.

> 1. [1.a] A memory module comprising:
>
> [1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
>
> [1.c] a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;
>
> [1.d] [1.d.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages, [1.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and [1.d.3] a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections, [1.d.4] wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and [1.d.5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.

Ex. 1001, 38:19–44.

F. Evidence

Petitioner relies on the following references (*see* Pet. 3, 9–14), as well as the Declaration of Dr. Andrew Wolfe (Ex. 1003).

Reference	Exhibit No.	Patent/Printed Publication
Harris	1023	U.S. Patent Pub. No. 2006/0174140 A1 to Harris, published Aug. 3, 2006
Amidi	1024	U.S. Patent No. 7,724,604 B2, issued May 25, 2010
Spiers	1025	U.S. Patent Pub. No. 2006/0080515 A1, published Apr. 13, 2006
FBDIMM Standards	1027, 1028	JESD82-20 and JESD205 standards published March 2007
Hajeck	1038	U.S. Patent No. 6,856,556 B1 to Hajeck, issued Feb. 15, 2005

G. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–30 are unpatentable on the following Grounds (Pet. 3):

Claims Challenged	35 U.S.C. §	References
1–3, 15	103(a)	Harris, FBDIMM Standards
1–30	103(a)	Harris, FBDIMM Standards, Amidi
1–30	103(a)	Harris, FBDIMM Standards, Amidi, Hajeck
1–30	103(a)	Spiers, Amidi
1–30	103(a)	Spiers, Amidi, Hajeck

II. ANALYSIS OF CHALLENGED GROUNDS

We now consider Petitioner's asserted grounds of unpatentability and Patent Owner's arguments to determine whether Petitioner has demonstrated by a preponderance of the evidence that the challenged claims would have been obvious under 35 U.S.C. § 103. *See* 35 U.S.C. § 316(e) (providing that

petitioner has the burden of proving unpatentability by a preponderance of the evidence).

A. Principles of Law

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination based on the teachings of multiple references requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see also KSR*, 550 U.S. at 418. Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418; *In re*

NuVasive, Inc., 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'").

B. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). "Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case." *Id.* at 696–97. The prior art may reflect an appropriate level of skill. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001).

Petitioner asserts a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field." Pet. 7–8 (citing Ex. 1003 ¶ 61). Petitioner contends that additional training can substitute for educational or research experience, and vice versa. *Id.* at 8. Petitioner asserts that such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols,

such as PCI and SMBus busses and protocols. *Id.* Petitioner further contends that such "a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers." *Id.* Petitioner further asserts that such "a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry." *Id.*

Patent Owner indicates "[f]or the purposes of this [Response], Patent Owner is applying the level of ordinary skill in the art proposed by Petitioner." Resp. 2.

The evidence that Petitioner presents mostly applies to the educational level and experience of workers in the field, but also touches upon other factors as well, including problems and solutions in the prior art and complexity of the technology. *See* Pet. 7–8. We find Petitioner's proposal is consistent with the level of skill in the art reflected by the '054 patent and the prior art of record, and, therefore, we adopt Petitioner's proposed level of ordinary skill in the art, with the exception of the open-ended language "at least," which introduces ambiguity and may encompass skill levels beyond ordinary.

C. Claim Construction

We construe claim terms "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2021). There is a presumption that claim

terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the specification. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Nonetheless, if the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor's lexicography governs." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing Phillips, 415 F.3d at 1312–17). Only disputed claim terms must be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

1. "Memory Module"

Patent Owner contends as follows:

> The term "memory module" appears in the preamble of the claims, and provides antecedent basis for the same term in the body of claims 1, 4, 6, 11, 16 and 25. The preamble is thus limiting as the District Court found after reviewing the specification in detail. Based on the intrinsic evidence, the Court also concluded that a memory module is a modular computer accessory that "includes the structure necessary to connect to a memory controller" of a host system.

Resp. 2–3 (citing Ex. 2032, 28). As support for its argument, Patent Owner quotes the District Court for the Eastern District of Texas as follows:

> While the claims recite many of the structural requirements of a "memory module," the claims arguably read on other modular computer devices, such as a video card or network controller, despite no evidence the inventors intended to encompass such devices by the claims. To the contrary, as the Overview section explains, the invention "is couplable to a memory controller of a host system," '918 Patent at 3:66–67 (emphasis added), not just the host system as recited in the claims. *See also id.* at 1:66–67 ("[t]he present disclosure relates generally to computer memory devices"). Thus, a skilled artisan would understand ***a "memory module" is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. That includes the structure necessary to connect to a memory controller***. *See* Memory Systems: Cache, DRAM, Disk [EX2034] … at 319 (depicting, in FIG. 7.6, a memory controller connected to two memory modules). Accordingly, the preambles are limiting.

Resp. 3 (citing Ex. 2032, 28) (emphasis in original). Patent Owner argues that Petitioner's expert, Dr. Wolfe, testified that the term "memory modules" typically refers to "main memory modules," which "are designed to connect to the primary memory controller for the purpose of holding general purpose code and data in a computer system." Resp. 3–4 (citing Ex. 2060, 123:14–25; Ex. 2056, 100:15–101:8 (by 2004–2005, a memory module "was intended to go into a dedicated memory slot and not a general-purpose IO slot")). Patent Owner contends that the '054 patent's usage of "memory module" is consistent with that understanding, and asserts that we should adopt the District Court's claim construction, including that the claimed "memory module" includes structures necessary to connect to a memory controller. *Id.* at 4 (citing Ex. 2061 ¶¶ 51–53).

In Reply, Petitioner contends that we properly found that Harris, the FBDIMM Standards, Amidi, and Spiers all disclose a "memory module" in

our Institution Decision. Reply 1–2 (citing Inst. Dec. 14–15, 17–18, 29–33, 47–48; Pet. 19–20, 77–78; Reply 24–27). Petitioner contends that the District Court's construction did not limit "memory module" to only "***main*** memory modules . . . designed to connect to the ***primary*** memory controller." *Id.* at 2 (emphasis in original) (citing Resp. 3–4). Petitioner contends that the District Court never used the words "main" or "primary," and that District Court's construction was simply that the "memory module" in the preamble was "limiting" without more. *Id.* (citing Ex. 2032, 26–28, 35). More specifically, Petitioner contends that the District Court did not further limit "memory module" to only "main memory modules . . . designed to connect to the primary memory controller." *Id.* at 2 (citing Resp. 3–4). Petitioner further contends that Patent Owner misleadingly quotes Dr. Wolfe's statements about "main memory modules," but asserts that Dr. Wolfe explained in the context of the '054 patent that a "memory module" is not limited to main memory or to any specific connection. *Id.* (citing Ex. 2060, 125:12–127:13 ("memory module" is a "circuit board that connects to a host computer that includes memory"); Ex. 2056, 100:15–101:19).

In Sur-Reply, Patent Owner disagrees with Petitioner's contention that "memory module" is not limited to "***main memory*** modules . . . designed to connect to the primary memory controller." Sur-Reply 1 (emphasis in original) (citing Reply 2). Patent Owner argues that Petitioner's contention "ignores the District Court's finding based on intrinsic evidence—which [Petitioner] did not object to—that "the invention [i.e., the claimed memory module] "is couplable *to a memory controller* of a host system," '918 Patent at 3:66–67 …, not just the host system as recited in the claims.'" *Id.* (citing

Ex. 2032, 28; Ex. 1001, 3:66–67, 4:5–12, 4:14–24, 4:35–39, 4:45–51, 5:4–20, 4:36–50, 6:4–6, 6:25–29, 6:61–66, 7:1–4, 7:21–25, 7:29–34, 7:43–49, 7:54–57, 21:24–25, 22:53–58, 23:19–22, 26:43–51, 23:41–44).

The District Court's Claim Construction Order (Ex. 2032) issued after our Institution Decision (Paper 11). Although Petitioner argued in the District Court litigation that the claim preambles were not limiting, Petitioner does not appear to maintain that argument here following the District Court's determination that the preambles are limiting. Ex. 2032, 35. Since the term is recited in both the preambles and bodies of these claims, there is evidence that the inventors of the '054 patent intended the term to limit the claim, as the District Court determined. *See Catalina Mktg. Int'l., Inc. v. Coolsavings,com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (citing *Bell Commc'ns Rsch., Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995) ("dependence on a particular disputed preamble phrase for antecedent basis may limit claim scope because it indicates a reliance on both the preamble and claim body to define the claimed invention.")).

We agree with Petitioner's contention that "memory module" is not limited to "***main*** memory modules . . . designed to connect to the ***primary*** memory controller." *See* Reply 2. The '054 patent states

> **In certain embodiments**, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the **main memory**.

Ex. 1001, 11:3–6 (emphases added). This is the only mention of "main memory" in the '054 patent. That the Flash memory serves as "main memory" in "certain embodiments" implies that there may be other embodiments in which this is not the case. Accordingly, we agree with

Petitioner that the term "memory module" is not limited to "***main*** memory modules . . . designed to connect to the ***primary*** memory controller."

We agree with Patent Owner that the "memory module" includes structure to connect with a "host system" including its memory controller. *See, e.g.*, Ex. 1001, code (57), 12:52–59. The claims do not mention a "memory controller," but they do mention that the "memory module" has an "interface" to connect with a "host system." Ex. 1001, 38:20–25 (claim 1), 39:63–65 (claim 16), 41:6–8 (claim 24). That the "memory module" has structure for connecting to the host system's memory controller may thus be implied from the claims.

We agree with Petitioner that the District Court's determination was that the preambles (presumably of claims 1, 4, 6, 11, 16 and 25) are limiting. Ex. 2032, 35. To the extent that the District Court's determination construed "memory module" to include structure necessary to connect to a memory controller, our construction of "memory module" is consistent.

D. Ground 1: Obviousness Over Harris and FBDIMM Standards

Petitioner contends claims 1–3 and 15 would have been obvious over the combination of Harris and FBDIMM Standards and relies on the Declaration of Dr. Andrew Wolfe (Ex. 1003) in support. Pet. 14–40. For the reasons that follow, we are persuaded that the evidence, including Dr. Wolfe's testimony, supports Petitioner's showing and establishes by a preponderance of the evidence that these claims are unpatentable.

1. Harris (Ex. 1023[2])

Harris is titled "Voltage Distribution System and Method for a Memory Assembly." Ex. 1023, code (54). Harris was published as U.S. Patent Pub. No. 2006/0174140 A1 on August 3, 2006. Petitioner contends Harris is prior art under § 102(a). Pet. 9.

Harris's Figure 1A is reproduced below.

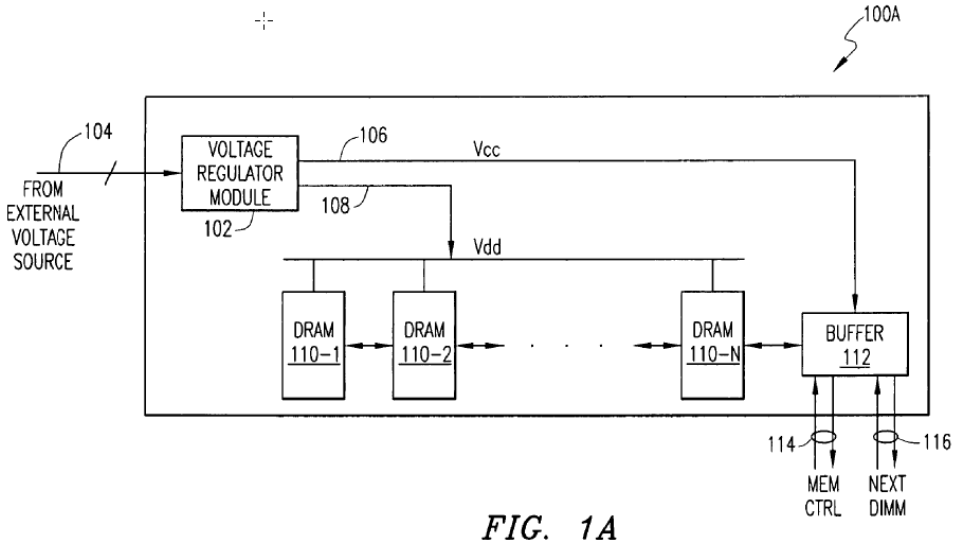


FIG. 1A

As shown in Figure 1A, Harris discloses a memory module 100A including on-board regulator 102 for converting an externally supplied voltage 104 to appropriate local voltage levels 106 (V_{cc}), 108 (V_{dd}), such as 0.5V to 3.5V. Ex. 1023, code (57), ¶¶ 9–10. Voltage 106 is supplied to buffer/logic component 112 which may be connected to a memory controller via interface 114 and daisy-chained with other memory assemblies via interface 116. *Id.* ¶ 9. Voltage 108 powers memory devices 110-1 to 110-N. *Id.* The memory module 100A may be a Dual In-Line Memory Module (DIMM)

[2] Exhibit 1023 is incorrectly identified in the Board's P-TACTS system as "Micron Tech., Inc. et al. v. Netlist, Inc., IPR2022-00418, Paper No. 2 (PTAB January 14, 2022) (831 Patent IPR Petition)," i.e., incorrectly repeating the identification provided for Exhibit 1022.

wherein each of the memory devices 100-1 to 100-N comprises a Double Data Rate (DDR), DDR2, or DDR3 device. *Id.* The memory module 100A may be an unbuffered, registered or fully buffered DIMM. *Id.*

2. FBDIMM Standards (Exs. 1027, 1028)

In March 2007, the Joint Electron Device Engineering Council (JEDEC) published standards for Fully Buffered DIMM (FBDIMM) memory modules titled "JESD82-20" (Ex. 1027) and "JESD205" (Ex. 1028). Ex. 1029 ¶¶ 134–137. Petitioner refers to these standards collectively as the "FBDIMM Standards." Pet. 10. Petitioner contends the FBDIMM Standards are prior art under § 102(a).

The FBDIMM Standards specify voltages for components on the memory module as follows:

Product Family Attributes

DIMM organization	x72 ECC			
DIMM dimensions (nominal)	30.35mm (height) x 133.35mm (width) x 8.2 mm (max thickness) MO-256 variation AB 30.35mm (height) x 133.35mm (width) x 8.8 mm (max thickness) MO-256 variation BB			
Pin count	240			
SDRAMs supported	256Mb, 512Mb, 1Gb, 2Gb, 4Gb			
Capacity	256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB			
Serial PD	Consistent with JC 45			
Supply voltages (nominal)	min	typ	max	
	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})
Buffer Interface	High-speed Differential Point-to-point Link at 1.5 volt			
DRAM Interface	SSTL_18			

Note 1: Approximate DC values, refer to AMB Component Specification for actual DC and AC values and conditions.
Note 2: Vtt range accomodates measurable offset due to complementary CA bus current paths. (See Vtt section)
An Unloaded system should supply Vtt of 0.48*Vdd/0.52*Vdd to Dimm socket

Ex. 1028, 9. The above table shows values for supply voltages including DRAM V_{DD}, AMB V_{CC}, DRAM interface V_{TT}, and V_{DDSPD}. The FBDIMM Standards further specify the following voltages for various power supplies:

Table 9.2 — Pin Description (Sheet 3 of 3)

Signal	Type	Description
$\overline{\text{RESET}}$	I	Power Good Reset
Miscellaneous Test		
TEST (4 pins)	NC	Pin for debug and test. Must be floated on DIMM.
TESTLO (5 pins)	A	Pin for debug and test. Must be tied to Ground on DIMM
TESTLO_AB20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
TESTLO_AC20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes
Other Pins		
BFUNC	I	**Buffer Function Bit:** When BFUNC = 0, AMB is used as a regular buffer on FB-DIMM. When BFUNC = 1, AMB is used as either a repeater or a buffer for LAI function. On FB-DIMM, BFUNC is tied to Ground
RFU (18 pins)	NC	**Reserved for Future Use.** Must be floated on DIMM. RFU pins denoted by "a" are reserved for forwarded clocks in future AMB implementations.
Other No Connect Pins		
NC (129 pins)	NC	No Connect pins

Ex. 1027, 83. The table above sets voltage levels for power supplies V_{CC}, V_{CCFBD}, V_{DD}, V_{SS}, and V_{DDSPD}.

3. Motivation to Combine

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Harris with the FBDIMM Standards with a reasonable expectation of success because Harris states that its Figure 1A may be a "fully buffered DIMM" (FBDIMM or FBD). Pet. 16 (citing Ex. 1023 ¶¶ 9–13; Ex. 1003 ¶¶ 158–166). Petitioner contends that a person of ordinary skill in the art would have understood that this type of DIMM is standardized in JEDEC's FBDIMM Standards and thus would naturally look

to them for more details about the "fully buffered DIMM" that Harris describes as compatible with the disclosed on-board voltage regulator module (VRM). *Id.*

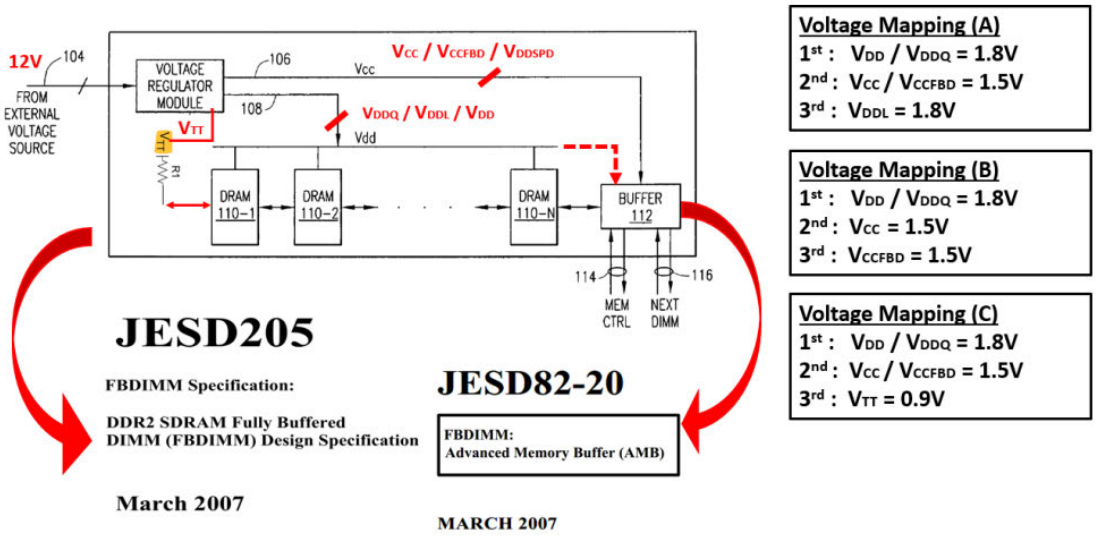
To explain its combination, Petitioner provides the following table:

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V

The table above shows Petitioner's Voltage Mappings A, B, and C from the FBDIMM Standards for Grounds 1–3, and how they disclose the "first," "second," and "third regulated voltages" in the claims. Pet. 27.

For Ground 1, Petitioner provides the illustration below:

Ground 1: Harris with JEDEC's FBDIMM Standards



This illustration shows how Petitioner is combining the teachings of Harris and the FBDIMM Standards to arrive at the claims. *Id.* at 15. Specifically,

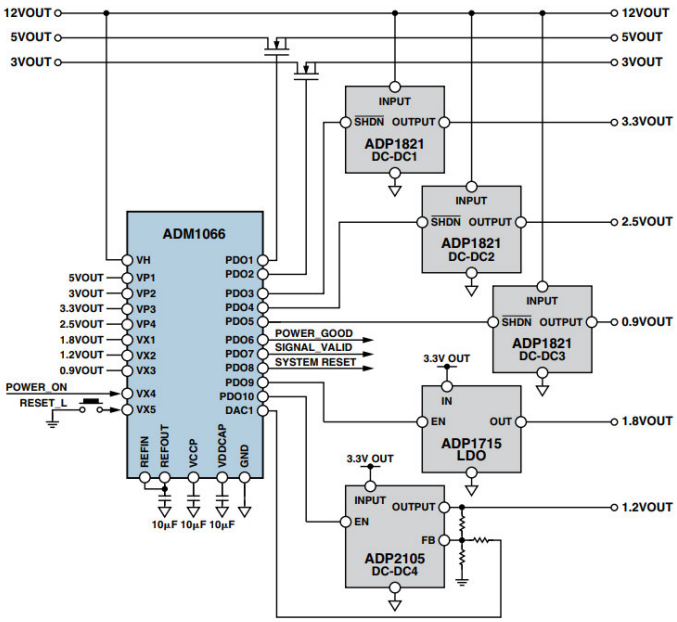
FBDIMM Standard JESD205 applies to Harris's memory module and JESD82-20 applies to the Harris's buffer. *Id.* at 26.

a) Modifying Harris to Have Three Converters

Patent Owner asserts that a person of ordinary skill in the art would not have modified Harris's memory module to have three converters, as Petitioner asserts. Resp. 18–20. Patent Owner contends that Petitioner did not demonstrate "a reason to modify Harris with the FBDIMM Standards," or "show a reason for Harris to use separate regulators for each of the alleged regulated voltages across all of Petitioner's Voltage Mappings A–C." *Id.* at 20. Patent Owner argues that it would not "have been obvious to use as many buck converters as possible, especially given that Harris expressly discloses a switching regulator outputting multiple voltage levels, consistent with the state of art." Sur-Reply 10–11 (citing Reply 11; Ex. 1023 ¶ 10; Ex. 2020, 5, Table 1-1). Patent Owner asserts that Petitioner "has not articulated any advantage of using one converter per voltage if Harris already uses a single converter for at least two voltages." *Id.* at 11 (citing Reply 11–14; Ex. 1023 ¶ 10).

As to why a person of ordinary skill in the art would use separate regulators for each of the voltages, Petitioner indicates that this was well-known in the art. Specifically, Petitioner contends that "buck converters were well-known switching devices commonly used to step down an input voltage to a lower output voltage." Reply 11 (citing Pet. 28–29; Ex. 1075, 103:21–107:14, 112:12–113:19). Petitioner contends that it "would have been obvious to a [person of ordinary skill in the art]—and consistent with Harris—to use three buck converters to convert the 12V input to the three required voltages on the memory board." *Id.* (citing Pet. 27–30; Ex. 2060,

53:16–54:14). Petitioner contends that "[t]his was common" as shown in the figure below:



Id. at 11–12 (citing Ex. 1062, 15, Fig. 4[3]). The above figure shows an ADM 1066 sequencer and three ADP182 DC-to-DC converters for generating 3.3V, 2.5V and 0.9 voltages outputs. Ex. 1062, 15. Petitioner also points to the data sheet for the ADP1821 titled "Step-Down DC-to-DC Controller," which describes a "synchronous, pulse-width-modulated (PWM), voltage-mode, step-down controller." Ex. 1078, 1; *see* Reply 11 (citing Ex. 1078, 1). Petitioner further relies on deposition testimony of

[3] Exhibit 1062 is titled "Analog Dialogue," Vol. 40, No. 2, published in 2006 by Analog Devices, Inc. "Analog Dialogue" contains several papers, one of which is titled "Power-Supply Management—Principles, Problems, and Parts" by Alan Moloney. The figure above was extracted from this paper. Although Exhibit 1062 was not identified in the Petition, it is part of the background knowledge that one of ordinary skill in the art would have had. *KSR*, 550 U.S. at 401 (obviousness analysis requires an assessment of the background knowledge possessed by person of ordinary skill in the art).

Patent Owner's expert, Dr. Mangione-Smith, who confirmed that the ADP1821 is a DC-to-DC converter and that it has structural elements and switching that are in common with buck converters to generate voltages. Reply 11 (citing Ex. 1075, 132:21–141:23). Patent Owner's argument that one of ordinary skill in the art would not have modified Harris to include three buck converters does not undermine Petitioner's showing of a motivation to combine Harris with the FBDIMM Standards when the background knowledge expressly teaches using three buck converters to generate voltages used in FBDIMMs. Pet. 16 (citing Ex. 1023 ¶¶ 9–13; Ex. 1003 ¶¶ 158–166); Reply 11–12 (citing Ex. 1062, 15, Fig. 4; Ex. 1078, 1).

Patent Owner argues that Harris's mention of "**a** high-frequency switching voltage regulator" means only one, and that Petitioner's contention that "a" means "one or more" applies to the claims, not the specification. Sur-Reply 11 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342–43 (Fed. Cir. 2008); Ex. 1023 ¶ 14). Patent Owner further argues that "Harris's reference to 'a high-frequency switching voltage converter capable of generating tightly-controlled voltage level**s**' (plural) means a single converter with multiple outputs, not multiple converters." *Id.* at 15–16 (citing Ex. 2061 ¶¶ 79–80).

Patent Owner does not address Petitioner's argument that Harris refers to "at least one on-board voltage regulator module (VRM)" in the specification and "at least one voltage regulator module" in claims 1 and 30. Reply 12 (citing Ex. 1023 ¶ 10, Fig. 1A). Patent Owner's argument does not undermine Petitioner's showing.

Patent Owner further asserts that space issues would have influenced any design decisions. Sur-Reply 12 (citing *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1368 (Fed. Cir. 2016)). Patent Owner argues there are good reasons why a person of ordinary skill in the art would have minimized the number of buck converters, including space constraints, and that Petitioner has not shown how multiple voltage converters would fit in the one square-inch space on both sides of the circuit board described as available for a voltage regulator module (VRM) in Harris. *Id.* at 12–13 (citing Ex. 1023 ¶ 13; Ex. 1078, 20–23; Ex. 2101, 22, 25–26).

Harris states that "[i]t is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board)." Ex. 1023 ¶ 13. Thus, Harris indicates that the VRM circuitry to generate two regulated voltages can fit within this space. Patent Owner argues that Petitioner's evidence shows that each ADP1821 converter package would be about 0.193 by 0.236 inches. Sur-Reply 12 (citing Ex. 1078, 20–23). This means three ADP1821 converters would occupy about 40% of the available space. Patent Owner does not demonstrate that the remaining 60% of available space would have been insufficient to accommodate the additional components required for three voltage converters. *Id.* at 12–13. In any case, we do not view Harris's disclosure of "approximately about one square inch" to limit the applicability of its teachings to a person of ordinary skill in the art. In the same paragraph, Harris states that the form factor "may be suitably modified." Ex. 1023 ¶ 13.

Patent Owner further argues that "independent voltage sources for different voltages would require specific control circuitry to delay and more precisely control each voltage source's ramping rate, adding complexity and cost without commensurate benefits." Sur-Reply 14 (citing Ex. 2061 ¶ 90). However, Dr. Wolfe states that it is simpler to use multiple regulators for multiple voltages since a single regulator that generates multiple voltages is more complicated than multiple regulators. Ex. 2060, 53:16–54:14, 89:1–21, *cited in* Reply 14. Dr. Wolfe further indicates that buck converters can be in some applications "extremely small." Ex. 2060, 89:11–15. Dr. Wolfe further testifies that multiple smaller converters may be less costly than a larger single converter because of component costs, separated spaces available for converters on circuit board, and other "ordinary engineering factors." *Id.* at 45:21–46:10.

Although Patent Owner may be correct that individual control of multiple voltage regulators would have required additional control circuitry, this does not meaningfully undermine the benefits that Petitioner mentions including permitting power sequencing, independent control of voltages, improved efficiency without generating excess heat or requiring cooling devices, and saving power. Pet. 29–30 (citing *id.* at 14–19; Ex. 1028, 17–20; Ex. 1026, 2–3, 9; Ex. 1028, 30–32; Ex. 1040, 1, 23–24 (Figs. 22–25); Ex. 1041, 1, 13; Ex. 1048, 3; Ex. 1058, 5; Ex. 1059, 5:23–30; Ex. 1062, 11, 13; Ex. 1064 ¶ 101; Ex. 1003 ¶¶ 240, 255). Dr. Wolfe testified that, in at least some circumstances, multiple converters may be less complicated, less costly, and take up less space. Ex. 2060, 45:21–46:10, 89:11–15. Patent Owner's argument that a single converter generating multiple voltages would be better in some circumstances does not negate that Petitioner's

proposed use of multiple converters for multiple voltages would have been preferred in other circumstances that a person of ordinary skill in the art would have recognized. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) ("Our caselaw is clear. It's not necessary to show that a combination is 'the *best* option, only that it be a *suitable* option.'" quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014)). Thus, Patent Owner's argument does not undermine Petitioner's showing of a motivation to combine Harris and the FBDIMM Standards.

b) Use of Separate Converters to Generate $V_{DD}/V_{DDQ}/V_{DDL}$ or V_{CC}/V_{CCFBD}

Patent Owner argues against Petitioner's showing of a motivation to combine by arguing that neither Harris nor the FBDIMM Standards suggest separate power rails for V_{DD}/V_{DDQ} and V_{DDL} or V_{CC} and V_{CCFBD} for Voltage Mappings A and B. Resp. 24–28. Patent Owner argues that the DDR2 Specification that Petitioner cited requires that the voltages V_{DD}, V_{DDQ} and V_{DDL} are driven from a single power converter output. *Id.* (citing Ex. 1026, 9; Ex. 2061 ¶ 87). The excerpt from the DDR2 Specification (JESD79-2B) in question states as follows:

2.3.1 Power-up and initialization sequence

The following sequence is required for POWER UP and Initialization.

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT*1 at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

Ex. 1026, 9 (DDR2); *see also* Ex. 1046, 15 (same for DDR3).[4] The above excerpt from the DDR2 Specification states a "first option" (boxed in blue[5]) that requires V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output, and a "second option" (boxed in red) the defines timings for when the voltages V_{DD}, V_{DDL} and V_{DDQ} must be applied relative to V_{DDL}, V_{DDQ}, and V_{TT} & V_{ref}, respectively. Patent Owner's argument focuses on the "first option" (boxed in blue above), which specifies that V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output. Resp. 24–28. However, Petitioner contends that the "second option" (boxed in red above) does not specify any converter. Petitioner contends that V_{DD}, V_{DDQ} and V_{DDL} would have been generated with separate converters because they are identified as separate voltages with separate pins (Ex. 1028, 17–20), JEDEC indicates that they can be turned on and off independently (Ex. 1026, 9), and JEDEC indicates that V_{DDL} should use an isolated voltage source (Ex. 1026, 2–3). Pet. 29–30 (citing Ex. 1003 ¶¶ 248–249; Ex. 1062, 13). Petitioner shows that one of ordinary skill in the art would have understood the second option

[4] Although Petitioner does not expressly rely on JEDEC's JESD79-2B (DDR2) (Ex. 1026) and JESD79-3A (DDR3) (Ex. 1046) in its combinations, the parties seem to be in agreement that these specifications are part of the background knowledge that a person of ordinary skill in the art would have had. In an obviousness analysis, the background knowledge is properly considered together with the demands known in the design community, and the inferences and creative steps that a person of ordinary skill in the art would employ. *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013).
[5] [5] In our opinion, Petitioner should have drawn the blue box to include the following two lines "VTT is limited to 0.95 V max, AND Vref tracks VDDQ/2" because of the way the standard presents the two sets of conditions with the word "or" between them and refers to them as "two sets of conditions." We refer to the two sets of conditions as "options" herein.

(boxed in red above) and other parts of the JESD78-2B specification suggest the possibility of using separate voltage regulators for V_{DD}, V_{DDQ} and V_{DDL}.

Patent Owner argues that a single power converter was required so that the voltages track one another during power up. Resp. 25–26 (citing Ex. 2006, 4; Ex. 2061 ¶ 88; Ex. 1023 ¶ 12). But Dr. Wolfe indicates that the voltages of separate converters can be made to track one another by coupling their feedback, which was a known option. Ex. 2060, 54:25–55:13. Patent Owner does not refute Dr. Wolfe's testimony.

Patent Owner asserts that Petitioner's contention that an FBDIMM has separate pins for V_{DD}, V_{DDQ} and V_{DDL} does not support its contention of separate converters, "particularly where it was known that there are stability and timing benefits when using a single source." Resp. 27 (citing Ex. 2006, 4). Dr. Wolfe explains that the FBDIMM module of Petitioner's combination would not have separate pins to receive V_{DD}, V_{DDQ} and V_{DDL} but would derive them onboard the module from the 12-volt input pin. Ex. 2060, 35:25–36:15. As to stability, Dr. Wolfe testifies that a feedback loop maintains stability in light of current variations, temperature changes, and other factors. *Id.* at 64:25–65:10. As to timing, Dr. Wolfe indicates that separate converters can track one another by coupling their feedback, and that this was a known option. *Id.* at 54:25–55:13.

Patent Owner argues that it was common for persons of ordinary skill in the art to supply all three voltages using a single power converter. Resp. 28 (citing Ex. 2060, 133:5–134:6, 39:11–40:24). Although using a single power converter may have been the most common approach, this does not negate Petitioner's showing that a person of ordinary skill in the art would have considered separate converters desirable under certain circumstances.

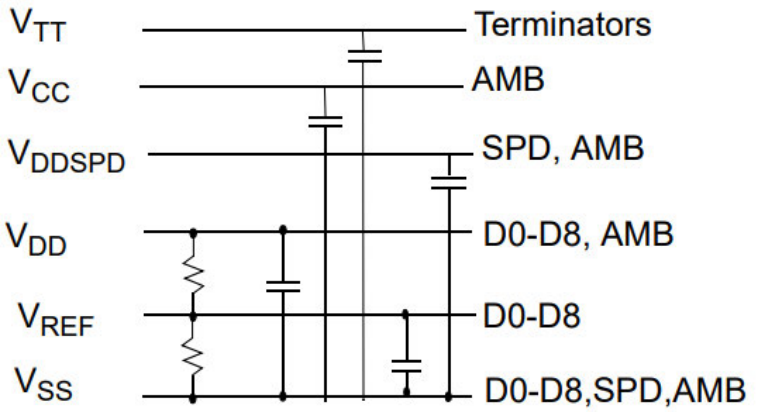
See Elekta Ltd. v. ZAP Surgical Systems, Inc., 81 F.4th 1368 (Fed. Cir. 2023) (quoting *Novartis Pharms. Corp. v. West-Ward Pharms. Int'l Ltd.*, 923 F.3d 1051, 1059 (Fed. Cir. 2019) ("Nor does an obviousness showing 'require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation . . . .'").

Patent Owner similarly argues that V_{CC} and V_{CCFBD} are separate voltages with separate pins, but asserts that Petitioner does not explain why a single on-board V_{CC} power source is insufficient for V_{CC} and V_{CCFBD} power rails when a single set of V_{CC} interface pins providing power from the host met the power needs for both V_{CC} and V_{CCFBD}. Resp. 29–30 (citing Pet. 30–31; Ex. 1028, 11–12; Ex. 2061 ¶ 92). For similar reasons as explained for V_{DD}, V_{DDQ} and V_{DDL}, we disagree. As Petitioner indicates, using separate converters for V_{CC} and V_{CCFBD} provides the benefits of sequencing the power, turning power on and off independently, saving cost, eliminating cross-coupling of noise, and solving space constraints. Reply 15 (citing Ex. 2060, 39:2–10, 44:25–46:10; Ex. 1075, 134:22–136:2, 194:23–195:7; Ex. 1062, 13–15; Ex. 2012, 73; Ex. 1003 ¶ 255).

Patent Owner's arguments do not undercut Petitioner's showing of a motivation to combine.

c) Motivation for Third Buck Converter for V_{TT}

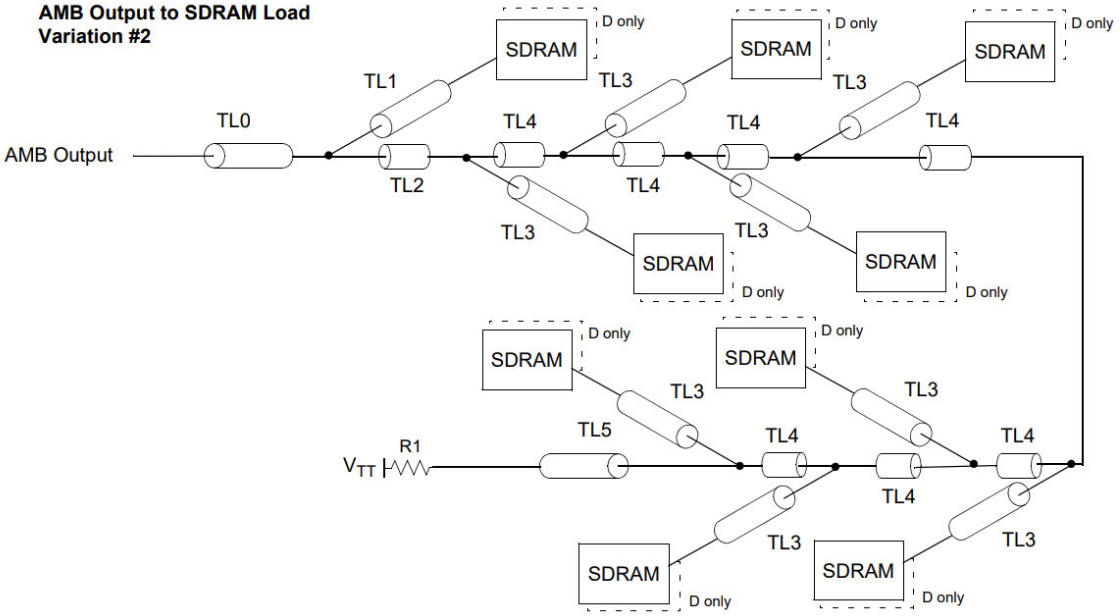
Patent Owner contends that Petitioner's Voltage Mapping C relies on three different voltages, including a termination voltage, V_{TT}, connected to terminators. Resp. 30 (citing Pet. 26; Ex. 1028, 13, 15–16). For context, the relevant figure from JESD205 is reproduced below:



Ex. 1028, 13. The above figure shows various voltages V_{TT}, V_{CC}, V_{DDSPD}, V_{DD}, V_{REF}, V_{SS} and their relationship to one another according to the JEDEC Specification JESD205. *Id.*

Patent Owner argues that Harris does not disclose generating V_{TT} on its module and argues that it would be supplied from the motherboard instead because this would ensure that all DIMMs have the same termination voltages and eliminate ground loops that could degrade signal integrity. Resp. 31–32 (citing Ex. 2061 ¶ 96). Patent Owner further argues that design complexity favors having a single regulator for a group of DIMMs rather than one regulator per DIMM. *Id.* at 32 (citing Ex. 1027, 20; Ex. 2061 ¶ 97; Ex. 2012, 72). In addition, Patent Owner argues that Petitioner touted JEDEC's move of voltage regulation from the motherboard to the DIMM as a "major design improvement" and Patent Owner asks, "If it had been so obvious, why did it take the industry so long to make that design improvement?" *Id.* at 32–33. Patent Owner further argues that generating V_{TT} is not one of two choices, and that V_{TT} is generally not provided to DDR2 modules; passive termination is used instead. *Id.* at 33 (citing Ex. 2061 ¶ 98; Ex. 2044, 6; Ex. 2045, 6; Ex. 2046, 4.20.11-6; Ex. 2006, 5).

In Reply, Petitioner argues that Harris teaches generating all of the voltages on the module, including all of the voltages for an FBDIMM, which would include V_{TT}. Reply 16 (citing Inst. Dec. 20–23; Ex. 1023 ¶ 12; Ex. 2060, 30:15–20, 72:22–73:7, 103:11–104:23, 109:5–111:10, 239:8–20). Petitioner contends that "Harris's module provides the voltages for the buffer 112 to send address and control signals to the DDR memory devices, which the FBDIMM Standards make clear require not just V_{DD}, but also V_{TT} to terminate those signals." *Id.* at 16–17 (underlining omitted) (citing Pet. 17–18; Ex. 1028, 9, 15, 68). Petitioner reproduces the figure below:



Pet. 17 (citing Ex. 1028, 68). The above figure is from the FBDIMM Standards and shows the net structure routing for addresses and commands from the advanced memory buffer (AMB) to the SDRAMs and how they are terminated by V_{TT}. *Id.* Petitioner contends that V_{TT} is required by the JEDEC Standards to track V_{DD} (Ex. 1028, 15) which is why dual buck converters for generating V_{DD} and V_{TT} were readily available. Reply 17–19

(citing Ex. 1028, 9; Ex. 2060, 72:22–73:7, 196:3–197:7; Ex. 1040, 1, 11; Ex. 1041, 1; Ex. 1048).

Petitioner further argues that Patent Owner's "suggestion of producing V_{TT} on the motherboard—where V_{TT} could change with each new generation of memory devices—would defeat the benefit of Harris's invention, e.g., 'a technology-independent voltage distribution scheme' to 'provide upgrades to next generation DRAM technology in a cost-effective manner.'" *Id.* at 19 (citing Ex. 1023 ¶¶ 2, 19).

We agree with Petitioner that the combination of Harris and the FBDIMM Standards at least suggests that V_{TT} can be generated onboard the memory module. Reply 16–19 (citing Pet. 17–18; Inst. Dec. 20–23; Ex. 1023 ¶¶ 2, 12, 19; Ex. 1040, 1, 11; Ex. 1041, 1–2, 7–9; Ex. 1048; Ex. 1075, 112:12–114:8; Ex. 2060, 30:15–20, 57:17–20, 58:18–59:10, 72:22–73:7, 103:11–104:23, 109:5–111:10, 140:15–24, 239:8–20). Harris indicates that its on-board voltage regulator converts externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module. Ex. 1023, code (57), ¶¶ 12, 16, Fig. 2, step 204. Petitioner shows that V_{TT} is needed onboard a memory module to terminate address and control signals. Reply 16–17 (citing Pet. 17–18; Ex. 1028, 9, 15, 68). In addition, Petitioner shows that V_{TT} is required by JEDEC to track V_{DD}, which is why dual buck converters for generating these voltages were commercially available. Reply 17–19 (citing Ex. 1028, 9; Ex. 2060, 72:22–73:7, 196:3–197:7; Ex. 1040; Ex. 1041; Ex. 1048). In light of these facts and the teachings of Harris and the FBDIMM Standards, Petitioner has shown that a person of ordinary skill in the art would have considered adding to the memory module a third buck converter to generate V_{TT}.

Patent Owner further argues that "even if V_{TT} is generated on module, there is no reason that it should be generated by a buck converter." Resp. 33. Patent Owner contends that, "[a]s Micron noted, an LDO would be sufficient to power V_{TT}." *Id.* (citing Ex. 2006, 7; Ex. 2007–2010; Ex. 2050). Patent Owner contends that an LDO is much smaller than a buck converter, including a controller and discrete components such as an inductor, which makes the LDO preferable given the space constraint. *Id.* (citing Ex. 2061 ¶ 99). Patent Owner also argues that an LDO is preferred when the current load is below 1A. *Id.* (citing Ex. 2061 ¶ 99; Ex. 2047, 21; Ex. 2048, 23; Ex. 2049, 20; Ex. 1040, 23–24, Figs. 22–25).

In Reply, Petitioner contends that buck converters were commercially available for V_{TT} and provided high efficiency compared to an LDO. Reply 19 (citing Ex. 1075, 112:12–114:8 (LDO may be only 10% efficient); Ex. 2060, 57:17–20, 58:18–59:10 (buck converters up to 98% efficient), 140:15–24 (trend has been to use buck converters)). We agree with Petitioner that, under appropriate circumstances, one of ordinary skill in the art would have chosen a buck converter over an LDO. Indeed, Patent Owner's arguments simply underscore that the person of ordinary skill in the art would have been aware of, and capable of using, various known options for voltage conversion.

d) Conclusion on Motivation to Combine Harris and the FBDIMM Standards

Petitioner has sufficiently shown that a person of ordinary skill in the art would have combined Harris and the FBDIMM standards since Harris states that its memory module may include fully buffered DIMMs (FBDs). Ex. 1023 ¶ 9. We agree that one of ordinary skill in the art would have

recognized this as a standard and looked to the FBDIMM Standards for information concerning the voltage values standardized for use in an FBDIMM. Ex. 1027, 83; Ex. 1028, 9. For these reasons and others set forth above, we determine that one of ordinary skill in the art would have combined Harris and the FBDIMM Standards with a reasonable expectation of success in arriving at the claims.

4. Analysis of Independent Claim 1

a) Limitation 1.a: "A memory module comprising:"

Petitioner asserts that Harris's memory module 100A in Figure 1A or memory module 306-1 in Figure 3 corresponds to the claimed "memory module." Pet. 19–20 (citing Ex. 1023 ¶¶ 9, 17, 20, Figs. 1A, 3; Ex., 1003 ¶¶ 217–223; Ex. 1028, 38). Harris does indeed disclose a memory module with multiple memory devices such as DRAMs 110-1 to 110-N in Figure 1A or 306-1 in Figure 3.

Patent Owner does not specifically respond to Petitioner's contention for the preamble. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has adequately shown that Harris teaches the preamble.

b) Limitation 1.b: "a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system"

Petitioner asserts that Harris and the FBDIMM Standards disclose this limitation. Pet. 20–25. For example, Petitioner notes that Harris discloses that its double-rank DIMMs may be accommodated on both sides of a printed circuit board (PCB). Pet. 20 (citing Ex. 1023 ¶ 13). Petitioner

further notes that a PCB may be referred to as a "memory board" or "raw card." *Id.* at 20–21 (citing Ex. 1023 ¶ 9, Ex. 1028, 10, 38, 84; Ex. 1003 ¶¶ 224–226).

As for the PCB "having an interface configured to fit into a corresponding slot connector of a host system," Petitioner notes that Harris's Figure 3 shows that each memory module 306-1 to 306-M includes an edge connection for fitting into a corresponding slot of a host system. Pet. 21 (citing Ex. 1023 ¶¶ 2, 12, 13, 19, Figs. 3, 4; Ex. 1028, 38, 84; Ex. 1003 ¶¶ 227–228).

Petitioner further contends that Harris, consistent with the FBDIMM Standards, discloses that the edge connections are "configured to couple power, data, address and control signals between the memory module and the host system." Pet. 21–25. Petitioner contends that the power signal corresponds to Harris's voltage 104 in Figure 1A (Ex. 1023 ¶ 10, 12, 19). Petitioner contends that the Harris's buffer 112 in Figure 1A is called "AMB" (Advanced Memory Buffer) in the FBDIMM Standards. Pet. 22. Petitioner indicates that buffer 112 receives data, address, and control signals via memory controller interface 114 and transmits these signals to DRAMs 110-1 to 110-N in Harris's Figure 1A. Pet. 22–25 (citing Ex. 1023 ¶ 9 (disclosing that "buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of memory devices 110-1 through 110-N")). In addition, Petitioner argues that the FBDIMM Standards indicate buffer AMB receives data signals DQ0–DQ63; address signals A0–A15; and control signals RAS, CAS, WE, CS, etc. Pet. 22–23 (citing Ex. 1028, 13).

(1) Power Via Edge Connection

Claim 1 recites "the interface including a plurality of edge connections configured to couple power . . . between the memory module and the host system." Ex. 1001, 38:22–25. Patent Owner argues that "all claims of the '054 patent require that the memory module includes a module interface that fits into a memory slot of a host system and receives voltage/power from the host system via that interface." Resp. 4–5. According to Patent Owner, Harris does not disclose such a memory module. *Id.* at 5. Specifically, Patent Owner argues that "Harris supposedly provides a 'technology-independent voltage distribution scheme for memory devices wherein system board power supply and associated voltage plane(s) are eliminated.'" *Id.* at 6 (citing Ex. 1023 ¶ 19) (emphasis omitted). Patent Owner argues that Harris's memory module connects to the external voltage source from the side and not from its edge connections. *Id.* at 7. Patent Owner contends that supplying power to a DIMM from its side was known in the art. *Id.* (citing Ex. 2035; Ex. 2036, 41–42; Ex. 2061 ¶ 59).

Petitioner contends that Patent Owner does not dispute that the FBDIMM Standards teach supplying power via edge connections, which Patent Owner's expert, Dr. Mangione-Smith, admits were "standard." Reply 3 (citing Pet. 16–21; Ex. 1075, 97:16–98:18, 163:16–20; Ex. 1077, 9). Petitioner further contends that Patent Owner argues that Harris's "externally supplied voltage" requires power external to the entire host system (*id.* (citing Resp. 4–8)), when "external" relates to the DIMM memory module and does not exclude power from the host system, including from edge connections. *Id.* (citing Ex. 2060, 66:7–19, 67:20–68:21, 91:22–92:7, 129:24–130:17; Pet. 21–22). Petitioner disagrees with

Patent Owner's assertion that Harris's memory module would never utilize edge connections for power. Reply 3–4. To explain its position, Petitioner provides an annotated version of Harris's Figure 3 below.

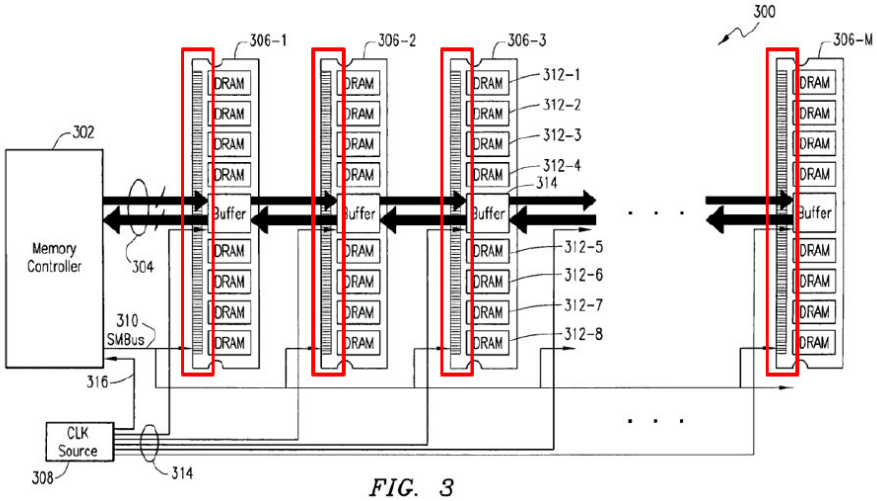


FIG. 3

Petitioner contends that Harris's Figure 3 above shows memory boards 306 connected to the host system only through their edge connections (annotated by Petitioner in red), implying that power would also come from those edge connections. Reply 4 (citing Ex. 1023, Fig. 3). Petitioner contends that Harris's Figure 3 is nearly identical to an Intel drawing where memory modules admittedly receive power through the edge connections from the host system. *Id.* (citing Ex. 1075, 171:3–17; Ex. 2101, 4).

Petitioner also contends that Harris discloses that each memory board receives a supply voltage which may be sourced from either the host system or a separate voltage source. *Id.* at 4–5 (citing Ex. 1075, 167:23–168:1; Ex. 1023 ¶ 17). Petitioner asserts that there is no dispute that the supply voltage was commonly provided through edge connectors alongside memory controller signals. *Id.* at 5 (citing Ex. 2060, 131:3–5).

We agree with Petitioner that Harris's "external voltage source" covers sources originating from the host system (as well as sources external

to the host system). Harris states as background that DRAM devices may be "powered from system board or main board voltage sources." Ex. 1023 ¶ 2. Harris also discloses that "external voltage sources may comprise any combination of *known* or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages." Ex. 1023 ¶ 14 (emphasis added). The parties agree that supplying power from a host system to a memory module was 'known' in the art, as referenced by Harris. Ex. 2060, 131:3–5; Ex. 1075, 162:18–25. And, as Petitioner notes, Harris's Figure 3 shows that the memory boards have only edge connections, suggesting they receive their power from them. Ex. 1023, Fig. 3; Ex. 1003 ¶ 229. These facts support the conclusion that Harris's external voltage source may originate from the host system. Accordingly, we do not agree with Patent Owner's arguments that Harris is limited to using only external voltage sources unrelated to the host system. Resp. 4–14; Sur-Reply 2–6.

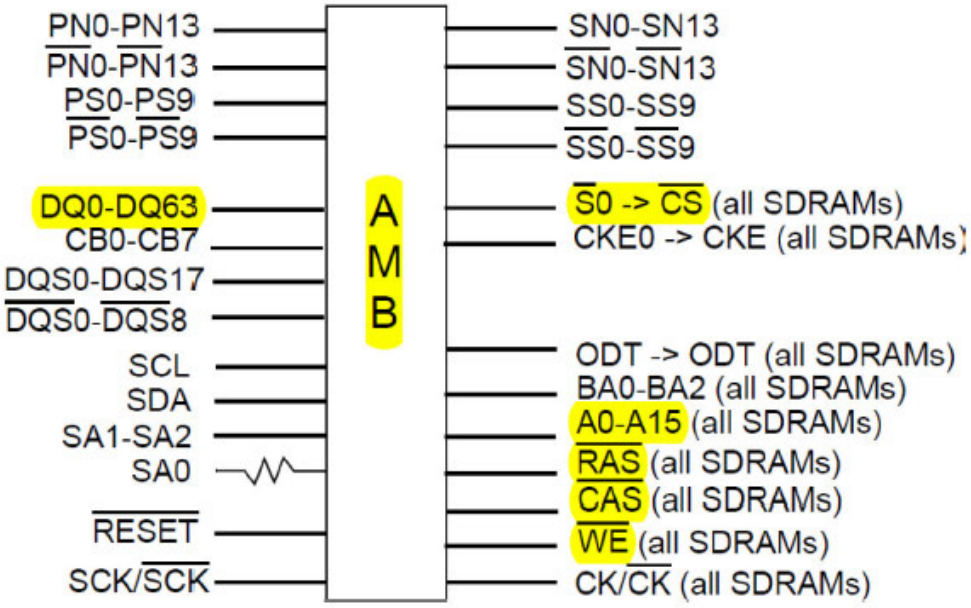
Furthermore, Petitioner demonstrates that the FBDIMM Standards show that memory modules receive power from their edge connections, and Petitioner relied on the FBDIMM Standards as disclosing this feature of the claims. *See* Pet. 16–21; Ex. 2060, 131:3–5; Ex. 1075, 97:16–98:18, 163:16–20; Ex. 1077, 9; Ex. 1028, 97 (GF-9), 103.

Based on our review and consideration of the record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards discloses this limitation.

(2) Data, Address, and Control Signals Via Edge Connection

Claim 1 recites an "interface including a plurality of edge connections configured to couple … data, address and control signals between the

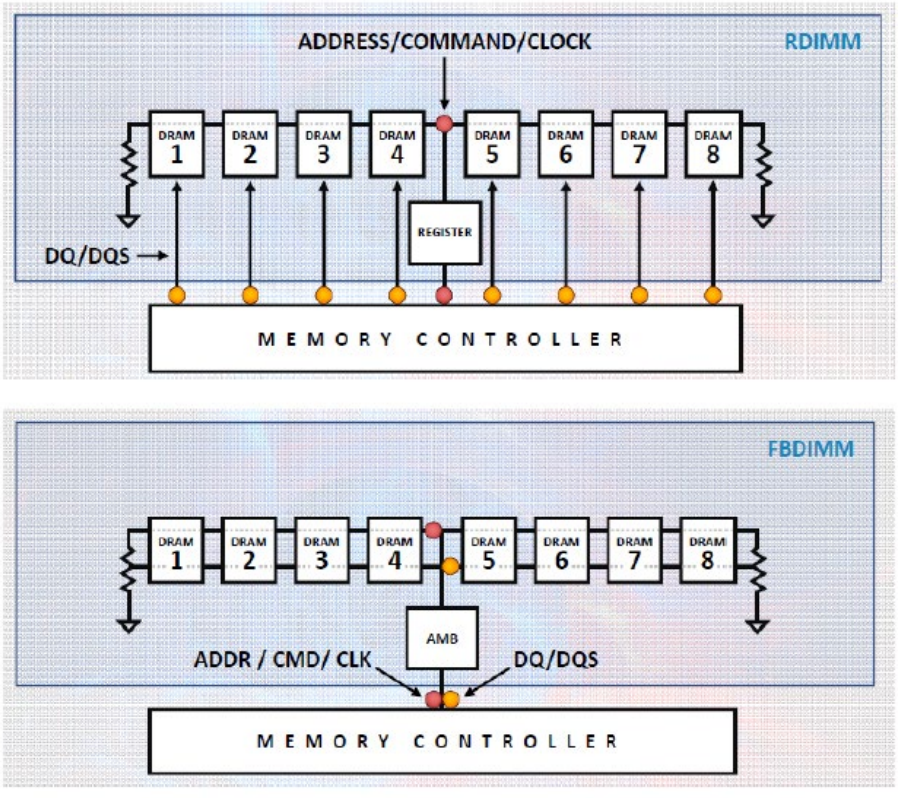
memory module and the host system." Ex. 1001, 38:23–25. Patent Owner argues that the DIMM and AMB do not receive data signals (DQ0–DQ63) or address and control signals (A0–A15, RAS, CAS, WE) from the host. Resp. 14 (citing Pet. 22–25). According to Patent Owner, these signals are instead generated by the AMB based on decoded FBDIMM channel signals (PS[9:0] and PS[9:0]bar). *Id.* at 14–18 (citing Ex. 2061 ¶ 72; Ex. 1028, 29; Ex. 1027, 3–4; Ex. 2039, 2; Ex. 2101, 4; Ex. 2040, 1). Patent Owner argues that Petitioner's evidence does not show that the data, address and control signals are received from the host. *Id.* at 18. Specifically, Patent Owner relies on the figure below from the FBDIMM Standards (*see* Sur-Reply 7 (citing Ex. 1028, 13)).



According to Patent Owner, the above figure shows that data, address and controls signals (highlighted in yellow) are generated and outputted by the buffer, and are not received from the DIMM interface. Sur-Reply 6–7 (citing Pet. 23–25; Resp. 14–18; Ex. 2061 ¶¶ 72–74). Patent Owner contends this does not comport with the claim language which requires an

"interface including a plurality of edge connections configured to couple … data, address and control signals between the memory module and the host system." *Id.* at 7 (citing Ex. 1001, 38:23–25). Patent Owner argues that Dr. Wolfe merely stated that the AMB outputs "information" to the DRAMs but the claims require specific "signals," not just "information." *Id.* at 8 (citing Ex. 1003 ¶ 230; Ex. 2060, 7:20–11:6; Ex. 1001, 38:23–25). Patent Owner argues that the outputs from the AMB are not transmitted over FBDIMM's edge connections. *Id.*

Petitioner argues that Patent Owner's technology tutorial indicates that an FBDIMM receives address and control signals similar to an RDIMM, as shown below:



Reply 9 (citing Ex. 1077, 8–9; Ex. 1075, 91:23–92:19, 95:14–96:13, 97:16–98:18). The figures above show that the memory controllers transmit

address, command and clock signals (shown in red), or information containing these signals, to the register (RDIMM) or AMB (FBDIMM), which transmits them to the DRAMs. *Id.*; Sur-Reply 10.

Petitioner contends that the host system provides address, command and clock signals to the AMB encoded as a packetized, serialized signal on fewer wires than would be required to receive them as separate, parallel signals. Reply 9–10 (citing Resp. 14; Ex. 2061 ¶ 31; Ex. 1075, 155:22–157:1, 212:3–8, 213:3–215:20, 219:13–220:9, 226:7–228:8; Ex. 2060, 8:3–11:6). Petitioner alleges that Patent Owner is in essence attempting to rewrite the claims to require dedicated pins for these signals, which the claims do not require. *Id.*

Patent Owner argues that it is not attempting to rewrite the claims to require "dedicated pins" as Petitioner alleges. Sur-Reply 9 (citing Reply 9–10). Patent Owner asserts that the pin names indicate what "signals" are exchanged at the interface between the host and the FBDIMM, as shown in the figure below.

Pin Name	Pin Description	Count
	FB-DIMM Channel Signals	99
SCK	System Clock Input, positive line	1
$\overline{SCK}$	System Clock Input, negative line	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{PN}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{PS}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{SN}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{SS}$[9:0]	Secondary Southbound Data, negative lines	10
FBDRES	To an external precision calibration resistor connected to Vcc	1
	DDR2 Interface Signals	175
DQS[8:0]	Data Strobes, positive lines	9
$\overline{DQS}$[8:0]	Data Strobes, negative lines	9
DQS[17:9]/DM[8:0]	Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.	9
$\overline{DQS}$[17:9]	Data Strobes (x4 DRAM only), negative lines	9
DQ[63:0]	Data	64
CB[7:0]	Checkbits	8
A[15:0]A, A[15:0]B	Addresses. A10 is part of the pre-charge command	32
BA[2:0]A, BA[2:0]B	Bank Addresses	6
$\overline{RASA}$, $\overline{RASB}$	Part of command, with $\overline{CAS}$, $\overline{WE}$, and $\overline{CS}$[1:0].	2
$\overline{CASA}$, $\overline{CASB}$	Part of command, with $\overline{RAS}$, $\overline{WE}$, and $\overline{CS}$[1:0].	2
$\overline{WEA}$, $\overline{WEB}$	Part of command, with $\overline{RAS}$, $\overline{CAS}$, and $\overline{CS}$[1:0].	2
ODTA, ODTB	On-die Termination Enable	2
CKE[1:0]A, CKE[1:0]B	Clock Enable (one per rank)	4
$\overline{CS}$[1:0]A, $\overline{CS}$[1:0]B	Chip Select (one per rank)	4
CLK[3:0]	CLK[1:0] used on 9 and 18 device DIMMs. CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use.	4
$\overline{CLK}$[3:0]	Negative lines for CLK[3:0]	4
DDRC_C14	DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.	1
DDRC_B18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_C18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_B12	DDR Compensation: Resistor connected to V_{SS}	1
DDRC_C12	DDR Compensation: Resistor connected to V_{DD}	1

Ex. 1028, 29. The figure above shows Patent Owner's highlighting to show the "FB-DIMM Channel Signals" including PS[9:0] and PS[9:0]bar, and the "DDR2 Interface Signals" including DQ0–DQ63, A0–A15, RAS, CAS, and WE. Patent Owner states that all memory control for the DRAM resides in the host, and argues that the fact that all read, write, and configuration accesses are addressed to the DIMM does not undermine that the signals Petitioner relies on are generated and outputted by the buffer, and not exchanged at the interface between the FBDIMM and the host. Sur-Reply 9–10 (citing Ex. 2060, 7:20–11:6; Ex. 2060 ¶ 230).[6]

[6] Patent Owner's citation to "Ex. 2060 ¶ 230" appears to be an error and we cannot determine from the context what Patent Owner intended to cite.

Petitioner further argues that the FBDIMM is a preferred embodiment in the '054 patent, and excluding a preferred embodiment from the claims is "rarely, if ever correct." Reply 10 (citing *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022)). To the contrary, Patent Owner argues that the claims need not encompass FBDIMM embodiments, which are disclosed but unclaimed subject matter. Sur-Reply 10 (citing *Maxwell v. J. Baker, Inc.*, 86 F.3d 1098, 1107 (Fed. Cir. 1996); Ex. 1001, 21:38–55).

According to Petitioner, Patent Owner concedes that the signals (PS[9:0] and PS[9:0]bar) received by the AMB result in data, address, and control signals needed by DDR2 SDRAMS. Reply 10 (citing Ex. 2061 ¶ 31). Petitioner further notes that the FBDIMM Standards state that all memory control for the DRAM resides in the host, including memory request initiation, and that the AMB acts as a DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM. *Id.* (citing Ex. 1027, 1). As a buffer for all such commands to the FBDIMM, Petitioner asserts, the AMB must necessarily couple data, address, and control signals from the host system to the memory module as the claims require. *Id.*

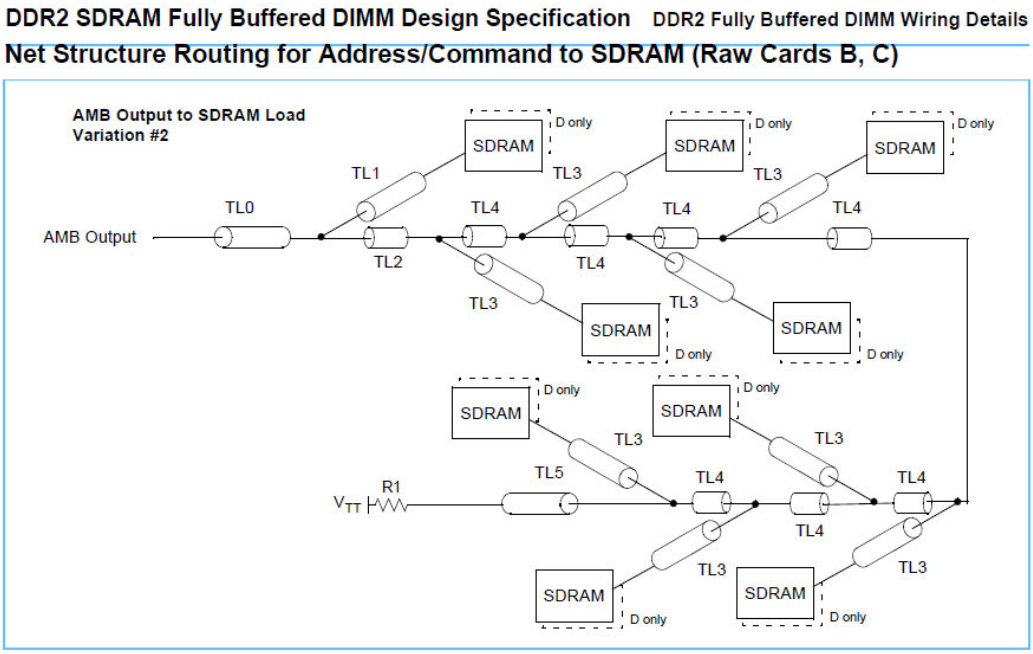
Petitioner and Patent Owner agree that FBDIMM AMB receives data, address, and control signals encoded in packetized, serialized form at its edge connections via the signals PS[9:0] and PS[9:0]bar, and that the AMB uses these signals to generate data, address and command signals including DQ0–DQ63, A0–A15, RAS, CAS, and WE provided to the DIMMs onboard the memory module. Pet. 22–25; Sur-Reply 10. The claims merely require an "interface including a plurality of edge connections configured to couple … data, address and control signals between the memory module and the host system." Ex. 1001, 38:23–25. We determine that the data, address, and

control signals of Harris and the FBDIMM Standards as received at edge connections coupling the memory module and host system satisfy this claim limitation, even though the signals are in encoded, packetized, or serialized form and thus may be received at the same pin or pins. That the signals are encoded, packetized, and serialized does not change the fact that they are data, address, and control signals. The claims do not require these signals to be received at the edge connections in any particular form or on any particular pins. *See In re Self*, 671 F.2d 1344, 1348 (CCPA 1982) (stating that limitations not appearing in the claims cannot be relied upon for patentability).

Petitioner has shown that the combination of Harris and the FBDIMM Standards teaches limitation 1.b of claim 1, and Patent Owner's arguments do not undermine Petitioner's showing.

> *c) Limitation 1.c: "a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages"*

Petitioner contends that Harris and the FBDIMM Standards disclose limitation 1.c of claim 1 of the '054 patent. Pet. 26–30. Specifically, Petitioner contends that Harris's Voltage Regulator Module 102 corresponds to the claimed "voltage conversion circuit." Pet. 26 (citing Ex. 1023 ¶ 10, Fig. 1A). Petitioner contends that the claimed "at least three regulated voltages" correspond to voltage 106 (V_{cc}) and voltage 108 (V_{dd}) as shown in Harris's Figure 1A, and a third voltage (V_{TT}) which is not actually shown in Harris's Figure but is shown in the FBDIMM Figure below.



Ex. 1028, 68. The figure above shows voltage V_{TT} terminating an array of SDRAM devices via resistor R1.

As to the voltages being "regulated," Petitioner argues Harris discloses that "at least one on-board voltage regulator" is "capable of generating tightly-controlled voltage levels." Pet. 28 (citing Ex. 1023 ¶¶ 2, 3, 9–11; Ex. 1003 ¶ 236).

As to the "at least three buck converters," Petitioner contends that Harris teaches using buck converters to provide the three regulated voltages above. Pet. 28 (citing Ex. 1003 ¶¶ 238–241). Petitioner contends Harris teaches using a "high-frequency switching voltage converter capable of generating tightly-controlled voltage levels" to provide each needed on-board regulated voltage. *Id.* (citing Ex. 1023 ¶¶ 10, 12). Petitioner contends it would have been obvious to use a "buck converter" to convert higher input voltage (e.g., 12V) to the lower output voltage (3.5V or less), and there would have been a reasonable expectation of success because buck

converters were well-known "switching" devices commonly used to step down the voltage between its input and output, as had long been taught in textbooks. *Id.* at 28–29 (citing Ex. 1003 ¶¶ 147–150, 239–241; Ex. 1058, 3, 5, 12–16 (1995 Lenk textbook showing buck, boost, and buck-boost circuits); Ex. 1032, 161 (1995 Mohan textbook showing various step-down (buck) converters); Ex. 1030, 2:32–43, 5:39–44; Ex. 1024, Fig. 6 (Amidi showing DC/DC buck converter); Ex. 1050, 1:21 (identifying buck converters as one of "the most basic building blocks in power electronics")). Petitioner contends buck converters were well-known for their efficiency in generating step down voltages without generating excess heat or requiring large cooling devices. *Id.* at 29 (citing Ex. 1003 ¶ 240; Ex. 1059, 5:23–30; Ex. 1058, 5; Ex. 1040, 1, 23–24; Ex. 1041, 1, 13; Ex. 1048, 3; Ex. 1062, 11; Ex. 1064 ¶ 101). Petitioner contends that it would have been obvious to use at least three converters in Harris given the need for at least three different voltages in the FBDIMM Standards. Pet. 29–30 (citing Ex. 1028, 17–20; Ex. 1026, 2–3, 9; Ex. 1003 ¶¶ 248–249, 255; Ex. 1062, 13; Ex. 1028, 30–32).

For the reasons discussed above in Section II.D.3, we disagree with Patent Owner's arguments regarding the use of three buck converters.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris and the FBDIMM Standards teaches limitation 1.c of claim 1.

d) Limitation 1.d.1: "a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages"

Petitioner asserts that Harris discloses a "a plurality of components coupled to the PCB" including a Buffer and DRAMs shown in Harris's Figure 3, and a Serial Presence Detect (SPD) and resistors. Pet. 31 (citing Pet. 14–19; Ex. 1003 ¶¶ 261–266). Petitioner further contends that these components are each coupled to at least one regulated voltage of the at least three regulated voltages. *Id.*

Patent Owner does not dispute that the combination of Harris and the FBDIMM Standards discloses this feature. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMMs Standards teaches limitation 1.d.1 of claim 1.

e) Limitation 1.d.2: "the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and"

Petitioner asserts that Harris discloses that the plurality of components includes a plurality of DDR DRAM devices 110-1 to 110-N as shown in Harris's Figure 1A and DRAM devices 312-1 to 312-8 for each of the memory modules shown in Harris's Figure 3. Pet. 31–32 (citing Ex. 1023 ¶¶ 9, 11, Figs. 1A, 3; Ex. 1003 ¶¶ 267–271). Petitioner contends that a person of ordinary skill in the art would have known that according to the JEDEC standards, DDR memory devices are "synchronous" DRAM devices. *Id.* (citing Ex. 1028, 9; Ex. 1045, cover; Ex. 1026, cover; Ex. 1046, cover).

Patent Owner does not dispute that the combination of Harris and the FBDIMM Standards discloses this feature. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris and the FBDIMMs Standards teaches this limitation.

> *f) Limitation 1.d.3: "a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections"*

Petitioner contends that the "first circuit" corresponds to buffer 112 as shown in Harris's Figure 1A, as well as the buffer of memory module 306-1 in Harris's Figure 3. Pet. 32–33 (citing *id.* at 20–25; Ex. 1023, Figs. 1A, 3; Ex. 1003 ¶¶ 272–277). Petitioner contends that Harris's buffers are coupled to receive data, address, and control signals via memory controller interface 114 across edge connections, and transmits them to DRAMs 110-1 to 110-N or DRAMs 312-1 to 312-8.

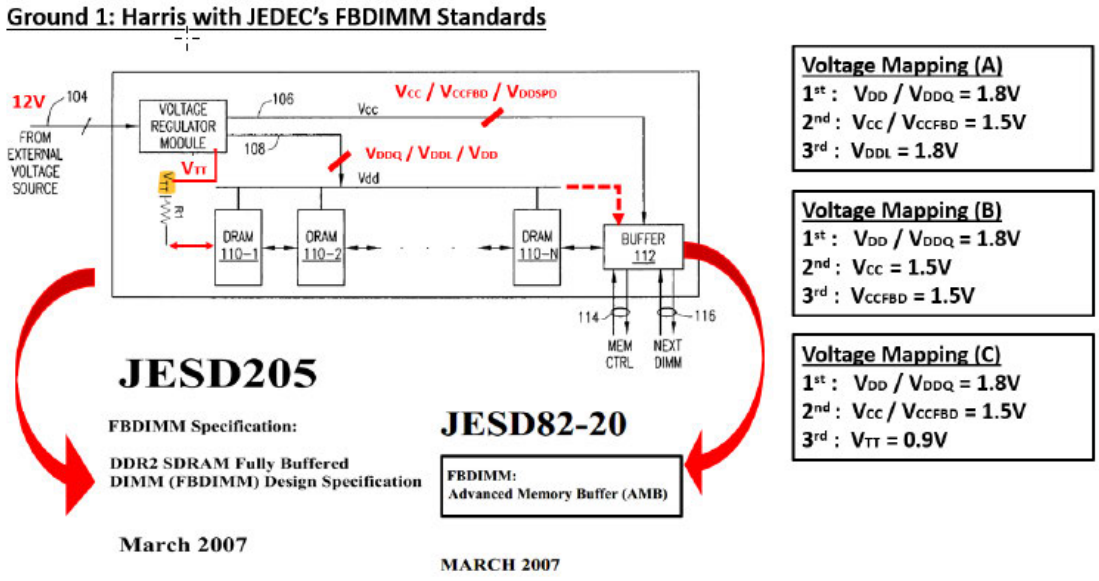
Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches this limitation for purposes of institution.

> *g) Limitation 1.d.4: "wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and"*

Petitioner contends that Harris's buffer corresponds to the first circuit and is coupled to "first" (e.g, V_{DD} or V_{DDQ} = 1.8V) and "second" (e.g., V_{CC} or V_{CCFBD} = 1.5V) "regulated voltages of the at least three regulated

voltages." Pet. 33–34 (citing *id.* 14–19, 27; Ex. 1003 ¶¶ 278–284). Petitioner provides an annotated version of Harris's Figure 1A shown below.



As shown above, Petitioner fills in Harris's Figure 1A with additional information from the FBDIMM Standards to show that Harris's buffer 112 would be understood by a person of ordinary skill considering the FBDIMM Standards to couple to the voltages V_{DD} or V_{DDQ} and V_{CC} or V_{CCFBD}.

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards teaches this limitation 1.d.4 of claim 1.

> *h) Limitation 1.d.5: "wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages"*

Petitioner contends that Harris with the FBDIMM standards discloses this limitation. Pet. 34 (citing *id.* 14–19, 27; Ex. 1003 ¶¶ 285–287). Specifically, Petitioner contends that the SDRAM devices from Harris's

Figure 1A are coupled to the first regulated voltage (V_{DD} or V_{DDQ} = 1.8V) of the "at least three regulated voltages." *Id.*

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Resp.

Based on our review and consideration of the record, we determine that Petitioner has shown that the combination of Harris with the FBDIMM Standards teaches limitation 1.d.5 of claim 1.

i) Conclusion for Claim 1

For the reasons explained in Section II.D.3, Petitioner shows that one of ordinary skill in the art would have had reason to combine Harris and the FBDIMM Standards with a reasonable expectation of success in arriving at claim 1. Furthermore, Petitioner has shown that the combination of Harris and the FBDIMM Standards teaches each limitation of claim 1. Accordingly, Petitioner has shown that claim 1 is unpatentable as obvious over the combination of Harris and the FBDIMM Standards.

5. Analysis of Dependent Claims

Claim 2 depends from claim 1 and recites "wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude, and wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes." Ex. 1001, 38:45–50. Petitioner contends that, as taught by the FBDIMM Standards, the first voltage amplitude may be 1.8V and the second voltage amplitude may be 1.5V which is less than the first voltage amplitude of 1.8V. Pet. 34–35 (citing *id.* at 14–19, 27; Ex. 1003 ¶¶ 288–296). Patent Owner presents no arguments specific to claim 2.

Claim 3 depends from claim 1 and recites "wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts." Petitioner contends that the third regulated voltage is V_{DDL} with a value of 1.8V as shown in the FBDIMM Standards (see previous figure—"voltage mapping (A)"). Pet. 35 (citing *id.* at 14–19, 27; Ex. 1003 ¶¶ 297–301).

Patent Owner argues that because claim 3 relies solely on Voltage Mapping A, Petitioner fails to show obviousness over the combination of Harris and the FBDIMM Standards. Resp. 28. Patent Owner argues that "[a]s for Mapping A, Petitioner does not explain why a single on-board Vcc power source is insufficient for [V_{CC}] and [V_{CCFBD}] power rails when a single set of [V_{CC}] interface pins providing power from the host met the power needs for both [V_{CC}] and [V_{CCFBD}]." *Id.* at 29. We addressed this argument in Section II.D.3.c explaining that Petitioner shows that using separate converters for V_{CC} and V_{CCFBD} provides the benefits of sequencing the power, turning power on and off independently, saving cost, eliminating cross-coupling of noise, and solving space constraints. We find no flaw in Petitioner's reliance on Voltage Mapping A for claim 3.

Claim 15 depends from claim 1 and recites "wherein two of the at least three buck converters are configured to operate as a dual-buck converter." Ex. 1001, 39:59–61. Petitioner contends at the time there were many commercially available products that could output two (or more) regulated voltages using buck converters, and thus "it would be obvious to implement any two of the regulated voltages as a '*dual buck converter*' to reduce the number of integrated circuits, pins, and interconnections on the module, therefore simplifying the design." Pet. 35–36 (citing Ex. 1003

¶ 439; *Qualcomm*, 21 F.4th at 797–99 (Fed. Cir. 2021)). Petitioner contends that the Murata MPD4S014S dual buck converter, Texas Instruments TPS51020 dual buck converter, and Fairchild FAN5026 dual-output PWM controller were commercially available and would have been suitable to implement for use in Harris in view of the FBDIMM Standards. Pet. 37–40 (citing Ex. 1003 ¶¶ 439, 443–444, 446–447; Ex. 1023 ¶ 10; Ex. 1032, 161–64; Ex. 1040, 1, 10–11; Ex. 1041, 1–2, 7–9; Ex. 1042, 16; Ex. 1047, 3:49–50, 4:7–10, 4:37–56, 5:4–13, 5:49–59, Fig. 2; Ex. 1048, 1–2; Ex. 1050, 2:19–20, 3:36–37; Ex. 1058, 5; Ex. 1073, 49–50, 58).

Patent Owner argues that claim 15 of the '054 patent provides "two of the at least three buck converters are configured to operate as a dual-buck converter," making clear that the "dual buck converter" includes two buck converters. Resp. 14 (citing Ex. 1001, 39:59–61). Patent Owner argues that Harris does not characterize its "high-frequency switching voltage converter" as a "dual" converter. *Id.* (citing Ex. 1023 ¶ 10, Fig. 1A). Patent Owner also contends Harris's use of the indefinite article "a" before mentioning this converter means that only a single converter is used in Harris's voltage regulator module. *Id.*

Petitioner correctly asserts that Harris states that "at least one on-board voltage regulator module (VRM)" may be used to generate the voltages V_{DD} and V_{CC}. Reply 12 (citing Ex. 1023 ¶ 10, Fig. 1A). Also, Harris's claims 1 and 10 recite "at least one voltage regulator module" which covers the possibility of multiple regulators. Although Harris expresses a preference for implementing a voltage regulator module using "a high-frequency switching voltage converter" (emphasis added) which may be understood to mean a single converter, Harris does not preclude using

multiple regulators to generate the voltages V_{DD} and V_{CC}. Ex. 1023 ¶ 10. As Petitioner states, Harris's voltage regulator module receives one input voltage and generates two output voltages. Reply 12 (citing Ex. 1023, Fig. 1A). One of ordinary skill in the art would have understood that there are two options: to use a single converter to generate both voltages, or to use multiple converters to generate the voltages. "When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 421. Petitioner shows that dual buck converters capable of generating the two voltages from the one input were known in the art and used for DIMMs, including the TPS51020 dual buck converter (Ex. 1040), the FAN5026 dual-output PWM controller (Ex. 1041), and the MPD4S014S dual buck converter (Ex. 1042). Armed with the foregoing knowledge, a person of ordinary skill in the art would have understood one option for implementing Harris's voltage regulator module would be to use a dual buck converter notwithstanding Patent Owner's arguments to the contrary.

Based on our review and consideration of the record, we determine that Petitioner has shown that Harris in combination with the FBDIMM Standards teaches the limitations of claims 2, 3, and 15.

6. Determination for Ground 1

Petitioner has shown that a person of ordinary skill in the art would have been motivated to combine Harris and the FBDIMM Standards with a reasonable expectation of success in arriving at the memory modules recited in claims 1–3 and 15. Accordingly, Petitioner has shown that claims 1–3

and 15 are unpatentable as obvious over the combination of Harris and the FBDIMM Standards.

E. Ground 2: Obviousness Over Harris, the FBDIMM Standards, and Amidi

Petitioner contends claims 1–30 of the '054 patent would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi. Pet. 41–70. For the reasons that follow, Petitioner shows by a preponderance of the evidence that claims 1–30 are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

1. Amidi (Ex. 1024)

Amidi was filed on October 25, 2006, issued on May 25, 2010, and is titled "Clock and Power Fault Detection for Memory Modules." Ex. 1024, codes (22), (45), (54). Petitioner contends Amidi is prior art under § 102(e). Pet. 11.

Amidi's Figure 5 is reproduced below.

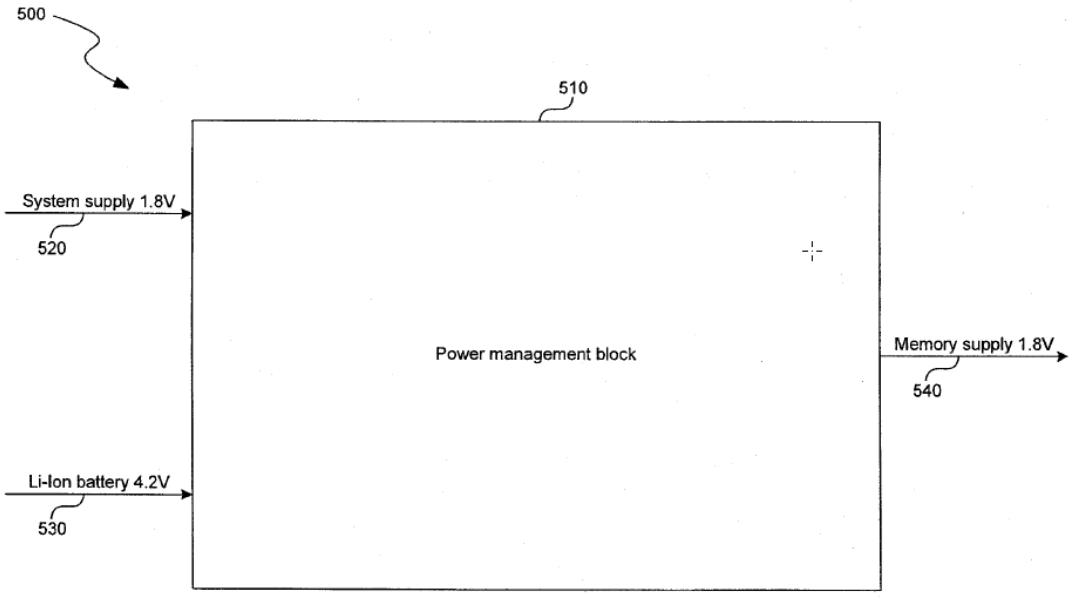


FIG. 5

Amidi's Figure 5 above illustrates power management block 510 that receives incoming system supply 520 and incoming battery supply 530, and generates outgoing memory power supply 540 which is stabilized in the face of disruptions to the system supply 520 using the battery supply 530. Ex. 1024, 4:14–22, 8:23–36, Fig. 5, Fig. 14; Ex. 1003 ¶¶ 131–132.

2. Motivation to Combine

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Harris and the FBDIMM Standards with Amidi with a reasonable expectation of success. Pet. 41. Specifically, Petitioner contends that Harris recognizes concerns with power reliability and proposes the use of a redundant power source. *Id.* (citing Ex. 1023 ¶¶ 12–14, 16, Figs. 1B, 2). Petitioner notes that Amidi teaches a redundant power source (a battery on the memory module) for maintaining data during power disruption. *Id.* at 41–42 (citing Ex. 1024, code (57), 1:28–35, 2:6–26, 4:14–60, Figs. 5–6; Ex. 1003 ¶¶ 171–177). Petitioner further notes that Amidi's power management block could be modified easily to work with Harris's FBDIMM memory module by changing the system supply 520 and memory supply 540 to 12V as taught by Harris. *Id.* at 42 (citing Ex. 1024, Fig. 5; Ex. 1023 ¶ 12; Ex. 1003 ¶¶ 173–174). According to Petitioner, a person of ordinary skill in the art would have considered it obvious that the 12V external supply would be stepped-down with a buck converter to a 5V supply for charging Amidi's battery and that Amidi's battery voltage would be stepped-up with a boost converter to the 12V level used by Harris's memory module. *Id.* at 42–43 (citing Ex. 1024, Fig. 6 (620); Ex. 1003 ¶¶ 173–174). Petitioner contends that Amidi discloses that its power management block uses "buck" converters to step-down voltages as needed,

and "boost" converters to step-up voltages as needed, as had long been taught in textbooks. *Id.* at 43 (citing Ex. 1024, 4:27–32, 4:38–40, Figs. 5, 6; Ex. 1058, 3; Ex. 1032, 161). Petitioner further contends that Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module and the FBDIMM standards, such that a person of ordinary skill in the art would have been motivated to combine their teachings. *Id.* at 43–45.

In sum, Petitioner contends that a person of ordinary skill in the art "would have been motivated to implement Harris's FBDIMM memory module with the functionality of Amidi's power management and logic blocks for detecting power disruptions and switching over to battery backup when needed." Pet. 44 (citing Ex. 1003 ¶¶ 171–176). Petitioner contends that this "straightforward modification of Harris's memory module in view of Amidi and the knowledge of a [person of ordinary skill in the art] simply uses a known technique (e.g., Amidi's battery backup techniques) to improve a similar device (e.g., Harris's memory module) in the same way (e.g., to provide a backup power supply using a battery)." *Id.* at 44 (citing Ex. 1003 ¶ 177); *see KSR*, 550 U.S. at 418. Petitioner further contends that "the modification merely applies a known technique (e.g., providing a backup power supply) to a known device (e.g., a memory module) that is ready for improvement to yield predictable results (e.g., redundancy when the system supply or clock fails)." Pet. 44 (citing Ex. 1003 ¶ 177); *see KSR*, 550 U.S. at 417.

Petitioner contends that the combination of Harris, the FBDIMM Standards, and Amidi would result in the following configuration and voltage mappings:

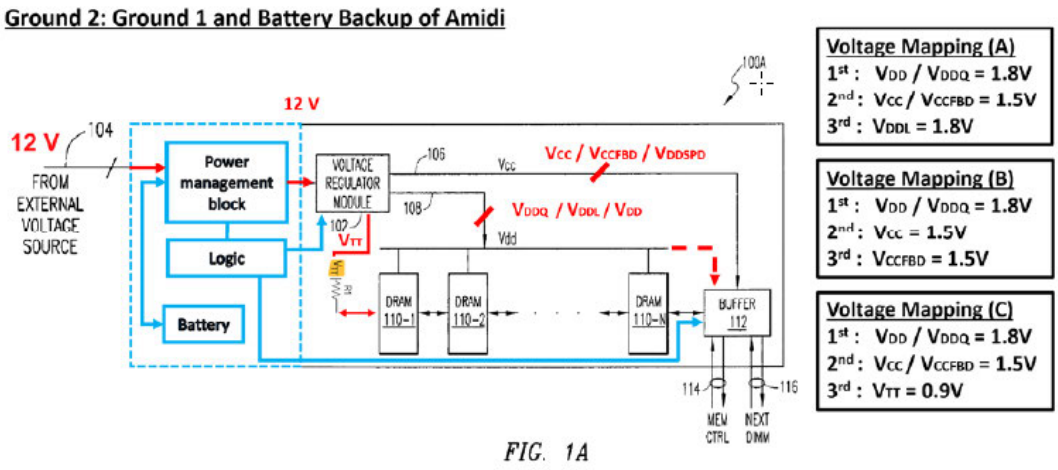


FIG. 1A

Pet. 45. Above, Petitioner has annotated Harris's Figure 1A to show features added from the teachings of the FBDIMM Standards (red) and features added from the teachings of Amidi (blue).

Patent Owner argues that Harris provides alternate voltage sources to power a memory module in the event of a power interruption, so Harris already provides a solution for the alleged problem that Amidi addresses. Resp. 34–40. Specifically, Patent Owner argues that Harris has "logic 124" that selects a different voltage source if power becomes unavailable on one of the supply voltage paths 120-1 through 120-K. *Id.* at 34–35 (citing Ex. 1023, Fig. 1B; Ex. 2061 ¶ 106). Patent Owner further argues that substituting Amidi's battery backup solution for Harris's redundant power sources would require substantial space to accommodate the lithium battery and associated battery charging and monitoring circuits and power management block. *Id.* at 37–38 (citing Ex. 1024, Figs. 4–6; Ex. 1023 ¶¶ 2, 13; Ex. 1061 ¶ 106, n.5; Ex. 2061 ¶ 107). Patent Owner argues that Petitioner "has entirely ignored the issue of whether the essential parts of Amidi it seeks to apply to the combination would even fit onto Harris' circuit board" and that "Petitioner has also presented no evidence that a

[person of ordinary skill in the art] would expect Harris' memory module to be able to accommodate three buck converters, a lithium battery and its associated charging and monitoring circuits, and Amidi's power management module, at least not without undergoing substantial red-design." *Id.* at 38–40 (citing Ex. 2101, 20; Ex. 1055, Fig. 4; Ex. 2061 ¶ 110).

We agree with Petitioner that Amidi provides a redundant power supply on the memory module that is independent from the host, and that a person of ordinary skill in the art would have seen the value of adding a redundant power supply onboard Harris's memory module at least for some practical applications. Reply 19–20 (citing Pet. 41–42; Ex. 1003 ¶ 172; Ex. 1024, 1:28–35, 2:6–26). Although Harris mentions an "external voltage source," it does not mention the term "battery." Hence, Patent Owner's arguments that Amidi provides a solution to a problem that Harris already solves is not correct. *See* Ex. 1003 ¶ 172 ("Amidi recognizes that it is useful to keep data on the memory module with a backup power supply on the module itself, such as a battery supply, when the entire system surrounding the memory module loses power") (citing Ex. 1024, 1:28–35; 2:6–26). Furthermore, Petitioner shows that memory modules with battery backup were known in the art and readily available. Reply 20 (citing Ex. 2035, 9; Ex. 1075, 165:10–167:7). As to the space issue, Petitioner notes that even if the battery backup occupies one side of an FBDIMM board, the other side still can include one rank or two ranks using stacked memory devices. *Id.* at 20–21 (Ex. 1028, 36; Ex. 1075, 74:22–75:25, 77:10–17).

Accordingly, we determine that Petitioner has shown that one of ordinary skill in the art would have been motivated to combine Harris, the FBDIMM Standards, and Amidi with a reasonable expectation of success.

3. Claims 1–3 and 15

We agree with Petitioner that the addition of Amidi does not negate Petitioner's showing with respect to the previous ground. Pet. 45–46 (citing Ex. 1003 ¶¶ 216–301, 431–448). Accordingly, Petitioner has shown that claims 1–3 and 15 are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi for the reasons stated in the previous ground.

4. Claim 4

Claim 4 depends from claim 1 and recites that the memory module further comprises:

> a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.

Ex. 1001, 38:54–64.

Petitioner points to Amidi's power supervisory module/block 480/665/800 as claim 4's "voltage monitor circuit" coupled to Harris's edge connections for power. Pet. 46. According to Petitioner, Amidi's power supervisory module/block monitors the external system power supply 605/825 in Amidi. *Id.* Petitioner contends that Amidi's power supervisory module/block generates a "trigger signal" corresponding to Amidi's signal

670/858/868. *Id.* Petitioner contends the "predetermined threshold voltage" corresponds to Amidi's reference voltage 675/820 set to 5% or 10% below the nominal voltage of 12V. *Id.* at 46–49 (citing Ex. 1023 ¶¶ 12, 13; Ex. 1003 ¶¶ 303–314; Ex. 1024, 4:8–11, 4:44–52, 5:25–43, 5:31–62, 8:30–62, 8:23–29, 9:8–12, Figs. 4–6, 14, 15). Petitioner further states that the trigger signal causes the memory module to transition from normal operations using an external voltage in the normal range ("the first operable state") to self-refresh operations using a backup battery when the external voltage is outside the normal range ("the second operable state"). *Id.* at 49–50 (citing Ex. 1024, 4:44–52, 8:30–62, 9:8–22, Figs. 6–8, 14, 15; Ex. 1003 ¶¶ 315–321).

Patent Owner does not present any argument specific to claim 4. *See* Resp.

Petitioner has shown by a preponderance of the evidence that claim 4 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

5. Claims 5, 7, 8, 23 and 24

Claim 5 depends from claim 4 and recites

> a controller coupled to the voltage monitor circuit;
> wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

Ex. 1001, 38:65–39:3. Claims 7, 23 and 24 recite the same or similar limitations. Petitioner contends that the combination of Harris, the FBDIMM Standards, and Amidi discloses these claims. Pet. 50–52 (claim 5); Pet. 55–57 (claim 8); Pet. 57–59 (claim 7); Pet. 69 (claims 23 and

24). We consider Petitioner's contentions and Patent Owner's arguments for claim 5 to be representative of the issues presented for all of these claims.

Petitioner contends that the logic for controlling the S3 sleep mode (Pet. 43–44) corresponds to the claimed "controller" that is coupled to the voltage monitor circuit (Amidi's voltage supervisory block). Pet. 50–51. Petitioner contends that "Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module, because both modes put the SDRAMs in a self-refresh state to preserve data while conserving power." Pet. 51 (citing *id.* at 43–44). According to Petitioner, "in the event of a power disruption causing Amidi's 'voltage monitor circuit' to produce a 'trigger signal' . . ., a [person of ordinary skill in the art] would have been motivated to use the S3 sleep mode discussed above . . . to conserve power when using Amidi's battery backup." *Id.* (citing Ex. 1003 ¶¶ 322–333). Petitioner contends that S3 configuration information is stored in non-volatile memory before entering the S3 sleep mode in response to the trigger signal, satisfying the "wherein" clause of claim 4 from which claim 5 depends. *Id.* at 51–52 (citing Ex. 1003 ¶¶ 322–340; Ex. 1027, 25, 117; Ex. 1028, 13; Ex. 1066, 26:64–27:4; Ex. 1067, 1–2; Ex. 1023 ¶ 19).

Patent Owner argues that each of these claims recites that the "controller" is part of the memory module. Resp. 46. However, according to Patent Owner, Dr. Wolfe stated that the S3 sleep mode is "always determined by something other than the memory module." *Id.* (citing Ex. 2060, 282:22–284:25; Ex. 2006, 3 (S3 controlled by main controller in CPU); Ex. 2061 ¶ 119. Patent Owner asserts that the memory controller outside of the memory module controls the S3 sleep mode, not a controller

onboard the memory module. *Id.* at 47 (citing Ex. 2061 ¶ 120); *see also* Sur-Reply 23–24.

Petitioner replies that Patent Owner's argument ignores the combination of Harris's FBDIMM S3 sleep mode with Amidi's teaching of backup power management and logic functionality on the memory module to "maintain memory (through refresh, for example)." Reply 23 (citing Pet. 43–44, 50–52; Inst. Dec. 35–36; Ex. 1024, 2:16–19, Fig. 11; Ex. 1003 ¶¶ 175–177). Petitioner contends that Amidi's logic disconnects the system memory controller from the module, so a person of ordinary skill in the art "would have been motivated to use the S3 mode of the buffer 112 [on Harris's module] when implementing the backup power supply and logic functionality as disclosed in Amidi, because S3 mode performs the function of refreshing the memory (e.g., self refresh), just like in Amidi." Ex. 1003 ¶¶ 329–330.

From the foregoing, it is clear that Petitioner is relying on Amidi's logic detecting a low voltage condition to initiate the S3 sleep mode of Harris's FBDIMM module, rather than a signal from the system memory controller. Petitioner otherwise shows the limitations of these claims are disclosed by the combination of Harris, the FBDIMM Standards, and Amidi.

Petitioner has shown by a preponderance of the evidence that claims 5, 7, 8, 23 and 24 are obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

6. Claims 6, 7, 9–12, and 17

Claims 6, 7, 9–12, and 17 recite, or depend from a claim that recites, that the voltage monitor circuit generates the trigger signal in response to the input voltage being above a predetermined threshold voltage. Ex. 1001,

39:4–20, 39:30–49, 40:21–25. We address Petitioner's contentions and Patent Owner's arguments for claim 6, which is representative of these claims.

Petitioner contends that claim 6 is similar to claim 4 except it concerns ***over***voltage detection rather than ***under***voltage detection as in claim 4. Pet. 52. Petitioner contends that Harris teaches to detect both undervoltage and overvoltage conditions. *Id.* at 53 (citing Ex. 1023 ¶ 13). In this regard, Harris states that the tolerance of the +12V power supply is "around +/- 15%." Ex. 1023 ¶ 13. Petitioner asserts that, in the combination, Amidi's power supervisory module/block 480/665/800 is coupled to Harris's edge connections for power. Pet. 53 (citing *id.* at 20–25). Petitioner further asserts that Amidi's signal 670/858/868 is the claimed "trigger signal" generated in response to the input voltage having an amplitude above the predetermined threshold voltage. Pet. 53 (citing *id.* at 46–49). Petitioner contends the predetermined threshold voltage corresponds to Harris's teaching of 15% above the nominal value of +12V, which is 13.8V. *Id.* (citing Ex. 1023 ¶ 13; Ex. 1003 ¶¶ 341–355).

Petitioner contends that Harris teaches both overvoltage and undervoltage detection of "+/- 15%." *Id.* (citing Ex. 1023 ¶ 13). Petitioner contends that a person of ordinary skill in the art would have been motivated by Harris to include overvoltage detection in Amidi's "voltage monitor circuit" with a reasonable expectation of success. *Id.* (citing Ex. 1003 ¶¶ 347–348). Petitioner contends that circuitry for both undervoltage and overvoltage detection was well known and commercially available. *Id.* at 54 (citing Ex. 1061, 15; Ex. 1062, 15; Ex. 1063, 1–2; Ex. 1065, code (57), ¶¶ 14, 18–19, Figs. 1, 5; Ex. 1003 ¶¶ 349–352).

As for the transition between the "first" and "second operable states," Petitioner contends that the "first operable state" in its combination is "e.g., normal operations using an external voltage when its amplitude is within a normal range," and the "second operable state" is "e.g., self-refresh operations using battery backup when the external voltage amplitude is outside the normal range." *Id.* at 54–55 (citing Ex. 1003 ¶¶ 356–359).

Patent Owner argues that neither Harris nor Amidi teaches detecting an overvoltage. Resp. 40. However, Harris discloses that its +12V power supply has a tolerance of "+/- 15%" which indicates it would be a concern if the power supply was greater than 15%. Ex. 1023 ¶ 13. Amidi indicates concern with "power faults." Ex. 1024, codes (54), (57). Although Patent Owner points out that Amidi discloses detection of undervoltage (Ex. 1024, Fig. 14), "power fault" is broad enough to encompass overvoltage as well. We agree with Petitioner that a person of ordinary skill in the art considering these teachings would have considered it obvious to detect overvoltage and generate a trigger signal to transition between operable states.

Patent Owner argues that the voltage regulators on which Petitioner relies do not detect input overvoltage because they can accommodate a wide range of input voltages, and there is a low probability that they would exceed their operational range. Resp. 42 (citing Ex. 2060, 58:24–61:12; Ex. 1040; Ex. 1041; Ex. 2061 ¶ 114). Petitioner replies that power surges were a known problem that could cause data loss or corruption or damage circuitry in memory boards. Reply 22 (citing Pet. 70–71; Ex. 1003 ¶¶ 138, 185). Petitioner contends that Harris discloses that its module can accommodate only "+/- 15%" of the nominal supply voltage, which is consistent with maximum ratings for commercial converters. *Id.* at 23

(citing Ex. 1041, 4). We agree with Petitioner that power surges would have been a problem in at least some circumstances for which one of ordinary skill in the art would have seen the value of voltage detection in order to take preventive action to avoid loss of data and damage to the memory module. Dr. Wolfe credibly explains that overvoltage was a danger known to persons of ordinary skill in the art, citing industry datasheets that specify overvoltage parameters. Ex. 1003 ¶¶ 351–352 (citing Ex. 1063, 1–2; Ex. 1061, 15; Ex. 1062, 15). Indeed, the cited evidence uses the phrase "an overvoltage fault" (Ex. 1061, 15), which shows that power faults are not limited to undervoltage situations.

On this record, we determine that Petitioner has shown that claims 6, 7, 9–12, and 17 are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi notwithstanding Patent Owner's arguments.

7. Claim 13

Claim 13 depends from claims 1 and 8, and recites "wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage." Ex. 1001, 39:50–54. Petitioner contends that claim 13 recites a limitation substantially similar to one addressed with respect to claim 4. Pet. 58 (citing Ex. 1003 ¶¶ 419–423). Patent Owner does not provide specific argument for claim 13. Petitioner has shown by a preponderance of the evidence that claim 13 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

8. Claim 14

Claim 14 recites

> wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.

Ex. 1001, 39:55–58.

Petitioner contends that a power disruption detected by Amidi's voltage supervisory block 800 causes the system to switch to battery backup. Pet. 61 (citing Pet. 55–57). Petitioner contends that Amidi's voltage supervisory block 800 detects a request by the host system to return control to the host. *Id.* at 61–62 (citing Ex. 1003 ¶¶ 424–430). Petitioner asserts that Amidi "discloses that, if the power is restored after a failure, the voltage supervisory block detects whether the host has cleared the backup-mode bit ('*detecting a request by the host system*') and subsequently, if so, returns control of the module to the host, including handling of the power signal." *Id.* at 62 (citing Ex. 1003 ¶¶ 311, 429; Ex. 1024, 5:31–62, 8:30–62, Fig. 14 9:11–39, Figs. 8, 14 (1460–1490), 15 (steps 1530, 1540, 1570, 1580; Ex. 1003 ¶ 312).

Patent Owner does not separately argue claim 14.

Petitioner shows by a preponderance of the evidence that claim 14 is unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

9. Claim 16

Petitioner contends that claim 16 is disclosed by the combination of Harris, the FBDIMM Standards, and Amidi for the reasons previously stated for claims 1, 8, and 9, noting that Amidi's voltage supervisory block (e.g., 665) ("the voltage monitor circuit") is "configured to detect an amplitude

change in the input voltage" when the external system supply changes by crossing the reference voltage. Pet. 58 n.4 (emphasis omitted) (citing Ex. 1003 ¶ 471).

Patent Owner presents no separate arguments for claim 16 apart from those previously discussed.

Petitioner has shown by a preponderance of the evidence that claim 16 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

10. Claims 18–22 and 26–28

Claim 18 depends from claim 16 and recites

> wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

Ex. 1001, 40:26–32. Claim 19 requires that the pre-regulated voltages are provided to the voltage conversion circuit "via a circuit." *Id.* at 40:33–37. Claim 20 recites that the "circuit" includes respective "first" and "second diodes" coupling respective "first" and "second pre-regulated voltages" to the "voltage conversion circuit." *Id.* at 40:38–46. Claims 21, 22, 27, and 28 recite limitations from claims that have been addressed or will be addressed in this section.

Petitioner contends that the limitation of claim 18 is taught by the combination of Harris, the FBDIMM Standards, and Amidi. Pet. 63–65. Petitioner contends that "pre-regulated voltage" means either that the voltage is within the 12V +/- 15% limits described in Harris, or must be pre-regulated on the memory board itself. Pet. 63; Ex. 1023 ¶ 13. We interpret

"pre-regulated voltage" to mean that the voltage is regulated before conversion to a stepped up or down level by the voltage conversion unit. *See* Ex. 1001, code (57), 28:53–58, Fig. 16 (1110, 1112). Petitioner contends that Harris discloses external voltage sources that are regulated. Pet. 63 (citing Ex. 1023 ¶¶ 13–14); *see* Ex. 1023 ¶ 14 ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages." (emphasis added)); Ex. 1003 ¶ 484. Thus, Harris's regulated voltage sources generate "pre-regulated voltages" as recited in these claims.

Petitioner contends that the combination discloses that in the first operable state, which is, for example, normal operation when the external voltage amplitude is within normal range, Amidi's voltage conversion circuit provides the first regulated voltage (V_{DD}/V_{DDQ}=1.8V) to the SDRAM devices. Pet. 63 (citing *id.* at 14–19, 27, 31–32, 45, 49–50; Ex. 1003 ¶¶ 480–487).

Petitioner further contends that the combination discloses that in the second operable state, which is, for example, self-refresh operations using battery backup when the external voltage amplitude is outside the normal range, Amidi's voltage conversion circuit provides the first regulated voltage to the SDRAM devices using a second pre-regulated voltage from a boost converter in the power management block that converts and pre-regulates the 4.2V battery voltage to the regulated output voltage of 12V. Pet. 65 (citing *id.* at 41–43, 49–50; Ex. 1003 ¶¶ 488–492).

For claim 19, Petitioner contends that the claimed "circuit" corresponds to the power switch multiplexer circuit shown in Amidi's

Figure 7 which supplies pre-regulated "System_VDD" in the first operable state (normal operation), and supplies pre-regulated and boosted "DC_18V" using the battery supply. Pet. 65–67 (citing *id.* at 26; Ex. 1023, Fig. 1A; Ex. 1024, 4:23–29, 4:56–5:24, Figs. 5–7; Ex. 1003 ¶¶ 493–500).

For claim 20, Petitioner contends that the first and second diodes as claimed are disclosed in Harris. Pet. 67–68 (citing Ex. 1024, 5:3 (first diode), 5:17 (second diode); Ex. 1024, 4:64–5:24, Fig. 7; Ex. 1003 ¶¶ 501–511).

For claims 21, 22, and 26–28, Petitioner relies on its contentions presented for claim limitations previously discussed. Pet. 68–70 (citing ¶¶ 450–452, 480–492, 494–500, 502–511, 513–526 (claim 21); ¶¶ 502–511; 527–530 (claim 22); ¶¶ 480–492, 571–576 (claim 26); ¶¶ 502–506, 577–580 (claim 27); ¶¶ 507–511, 581–584 (claim 28)).

Patent Owner does not present any arguments specific to these claims.

After reviewing the record, we determine that Petitioner has shown by a preponderance of the evidence that claims 18–22 and 26–28 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

11. Claim 25

Petitioner contends that the limitations of claim 25 were addressed with respect to claims 4 and 16. Pet. 58, 70.

Patent Owner provides no argument specific to claim 25. *See* Resp.

Petitioner has shown by a preponderance of the evidence that claim 25 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

12. Claim 29

Claim 29 depends from claim 24 and recites that the voltage monitor circuit is configured to detect whether the input voltage is above or below respective thresholds. Ex. 1001, 42:19–23. Petitioner contends that the limitations of claim 29 were addressed with respect to claims 4, 6, and 17. Pet. 58, 70.

Patent Owner provides no argument specific to claim 29. *See* Resp.

Petitioner has shown by a preponderance of the evidence that claim 29 is obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

13. Claim 30

Claim 30 depends from claim 29 and recites that the predetermined threshold voltages are above and below a "specified operating voltage." Ex. 1001, 42:24–27. Petitioner contends that the "specified operating voltage" corresponds to Harris's +12V nominal external voltage. Pet. 57 n.2 (citing Pet. 41–45; Ex. 1023 ¶¶ 12, 13).

Patent Owner does not present any arguments specific to claim 30. *See* Resp.

Petitioner has shown by a preponderance of the evidence that claim 30 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

14. Determination for Ground 2

Petitioner has demonstrated that a person of ordinary skill in the art would have had reason to combine Harris, the FBDIMM Standards, and Amidi with a reasonable expectation of success. Petitioner has also demonstrated that all of the limitations are taught or at least suggested by the

combination. Accordingly, under this ground, Petitioner has demonstrated by a preponderance of the evidence that claims 1–30 are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

F. Ground 3: Obviousness over Harris, the FBDIMM Standards, Amidi, and Hajeck

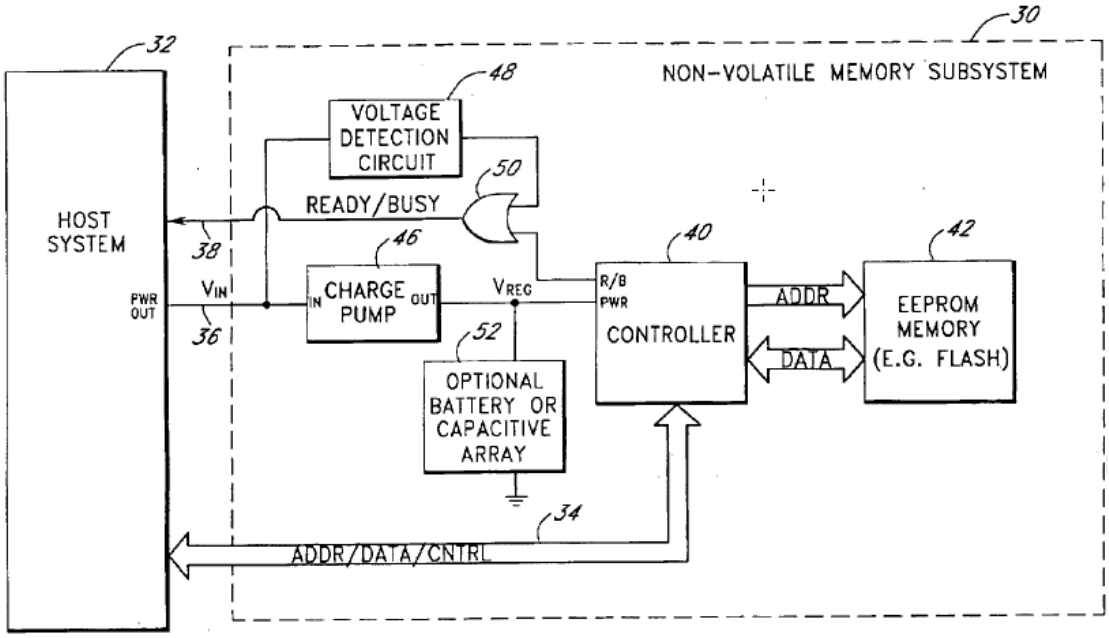
Petitioner contends claims 1–30 would have been obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck. Pet. 70–72.

1. Hajeck (Ex. 1038)

Hajeck is titled "Storage Subsystem with Embedded Circuit for Protecting Against Anomalies in Power Signal from Host." Ex. 1001, code (54). Hajeck issued as U.S. Patent No. 6,856,556 B1 on February 15, 2005. Petitioner contends Hajeck is prior art under § 102(b). Pet. 12.

Hajeck seeks to protect storage subsystems from damage and data loss caused by irregularities in a power signal provided by a host. Ex. 1038, 1:10–13. Specifically, Hajeck seeks to prevent data loss due to loss of power from a host system, and to prevent power surges or spikes from damaging circuitry of the storage subsystem. *Id.* at 1:15–31.

Hajeck's Figure 1 is reproduced below.



In Hajeck's Figure 1, non-volatile memory subsystem 30 receives power from host system 32 at charge pump 46 which supplies regulated voltage to controller 40. *Id.* at 2:64–67. In the event of a power surge or spike, charge pump 46 protects controller 40 from damage. *Id.* at 3:12–16. In the event of a voltage drop, charge pump 46 with battery and capacitive array 52 provides sustained voltage to controller 40. *Id.* at 2:60–63, 3:10–13. Voltage detection circuit 48 detects anomalies in the input voltage and generates a "busy" signal provided to the host system 32 to block the host system from performing write operations to the storage subsystem. *Id.* at 1:64–67, 3:30–33.

2. Motivation to Combine

Petitioner contends that one of ordinary skill in the art would have been motivated to combine Hajeck with Harris, the FBDIMM Standards, and Amidi because one would have appreciated the desirability of switching to backup power in both undervoltage and overvoltage conditions.

Pet. 71–72. Hajeck teaches using a battery backup in response to power loss from the host system to complete outstanding operations and to use the charge pump to protect the controller from surges or spikes in the power supply. *See, e.g.*, Ex. 1038, code (57). Hajeck also teaches a voltage detection circuit generate a "busy" signal in response to undervoltage or overvoltage conditions. *Id.* at 3:30–43.

3. Claims 7, 9–12, 17, 29, and 30

Petitioner asserts that claims 1–30 would have been obvious under this ground for the same reasons provided for Ground 2. Pet. 71 (citing *id.* at 45–70). Petitioner contends that to the extent one would argue that Ground 2 fails to teach ***over***voltage detection, Hajeck discloses this feature. Pet. 71 (citing *id.* at 52–54). Specifically, Petitioner contends that Hajeck discloses overvoltage detection as required by claims 7, 9–12, 17, 29, and 30. Pet. 71 (citing *id.* at 52–54; Ex. 1003 ¶¶ 354–355). Petitioner contends a person of ordinary skill in the art would have looked to Hajeck's teachings about voltage anomalies when implementing Amidi's voltage supervisory block to detect both undervoltage and overvoltage anomalies. *Id.* at 71–72 (citing Ex. 1003 ¶¶ 186–188). In the combination, "Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only '[i]f system supply 605 has a magnitude lower than reference voltage 675' as disclosed by Amidi (Ex. 1024, 4:44–52), but also 'when the voltage exceeds a certain level' as taught by Hajeck (Ex. 1038, 3:30–43; *see also id.* at code (57), 1:10–18, 1:28–31, 1:62–2:7, 3:30–4:9, 4:62–65, Fig. 1)." *Id.* at 72. Petitioner contends that this ground teaches both overvoltage and undervoltage detection and protection, further

rendering obvious claims 6, 9, 17, and 29 and their dependent claims 7, 10–12, and 30. *Id.* (citing Ex. 1003 ¶¶ 354–355, 389, 478, 588).

Patent Owner argues that "Harris does not teach the need to detect undervoltage and overvoltage anomalies" and that Hajeck "does not teach or suggest a voltage detection circuit that produces a trigger signal that causes transitions to different operating states in over-voltage conditions or otherwise even relates to switching power sources" or "sending the trigger signal to the memory system." Resp. 42–43 (citing Pet. 48, 51). Patent Owner argues that "the only signal generated by Hajeck's voltage detection circuit 48 is a 'busy signal' 38 sent back to host 32 to prevent it from performing write operations to the memory subsystem 30 when voltage anomalies are detected." *Id.* at 43 (citing Ex. 1038, 3:30–57, Fig. 2). Patent Owner argues that Hajeck does not switch to a different operating state or a different power supply, but instead its charge pump 46 continues to provide a near-constant voltage V_{REG} to controller 40. *Id.* (citing Ex. 1038, 3:6–10, 3:66–4:3; Ex. 2061 ¶ 116). Patent Owner argues that Hajeck's charge pump protects controller 40 and other circuits from damage caused by voltage surges and spikes. *Id.* at 44 (citing Ex. 1038, 4:7–9).

Petitioner replies that Patent Owner's arguments ignore the Petition's extensive explanation and evidence about a person of ordinary skill in the art's understanding of how to handle power anomalies, including both undervoltage and overvoltage conditions, with a reasonable expectation of success. Reply 21 (citing Pet. 12–13, 41–45, 53–54, 70–72; Ex. 1003 ¶¶ 138, 345–355). Petitioner contends that the Petition also explained how the combination teaches a trigger signal to switch to back-up power and avoid data loss in case of a "power fault" including undervoltage and

overvoltage conditions. *Id.* (citing Pet. 49–50; Ex. 1003 ¶¶ 315–321; Ex. 2060, 226:16–22, 230:17–232:6, 251:10–254:2).

We agree with Petitioner that Patent Owner's arguments attack the references individually and do not properly consider what the combination of references would have signified to a person of ordinary skill in the art. *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)). Petitioner relies on Hajeck for its teaching of detecting an overvoltage condition to the extent that the combination of Harris, the FBDIMM Standards, and Amidi were deemed not to already disclose that feature. Pet. 72 (citing Ex. 1038, 3:37–40). Thus, the features that Patent Owner argues are missing from Hajeck are not ones for which Petitioner relied on Hajeck.

For similar reasons, we also do not agree with Patent Owner's argument that Hajeck does not suggest that data loss was a concern because its charge pump could provide the desired V_{REF} indefinitely. Resp. 44–45. Petitioner relies on Amidi for switching operational states and the voltage supply to battery backup in the event of an overvoltage. Reply 21 (citing Pet. 49–50). This argument also considers Hajeck individually, and not in combination with Harris, the FBDIMM Standards, and Amidi, as set forth in the Petition.

4. Determination for Ground 3

Petitioner has shown that a person of ordinary skill in the art would have combined Harris, the FBDIMM Standards, Amidi and Hajeck with a reasonable expectation of success. Petitioner has also shown that all of the limitations of claims 1–30 are taught or at least suggested by the combination. On this record, Petitioner has shown by a preponderance of

the evidence that claims 1–30 of the '054 patent would have been obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck.

G. Grounds 4 and 5: Obviousness over Spiers and Amidi

As we have determined that claims 1–30 are unpatentable as obvious under Grounds 1 to 3, we do not reach Grounds 4 and 5.

H. Motion to Exclude

Petitioner seeks to exclude materials referenced in three URLs submitted with Patent Owner's Sur-Reply on August 4, 2023. Paper 35 (citing Paper 33, 1 n.2, 24, 26). Because we do not rely on any of these URLs in a manner adverse to Petitioner, we dismiss the Motion to Exclude as moot.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner establishes by a preponderance of the evidence that claims 1–30 of the '054 patent are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1–30 of the '054 patent have been shown to be unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed as moot;

FURTHER ORDERED that Petitioner will contact the Board within seven (7) business days to correctly identify Exhibit 1023 as Harris in the Board's P-TACTS system.

FURTHER ORDERED that any party seeking judicial review must comply with the notice and service requirements of 37 C.F.R. § 90.2.[7]

[7] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1–3, 15	103	Harris, FBDIMM Standards	1–3, 15	
1–30	103	Harris, FBDIMM Standards, Amidi	1–30	
1–30	103	Harris, FBDIMM Standards, Amidi, Hajeck	1–30	
1–30	103	Spiers, Amidi[8]		
1–30	103	Spiers, Amidi, Hajeck		
Overall Outcome			1–30	

[8] Because we determine that claims 1–30 are unpatentable on other grounds, we do not reach the remaining grounds.

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